DESIGN AND ANALYSIS OF LOG-DOMAIN FILTERS USING THE E-CELL APPROACH

By

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DESIGN AND ANALYSIS OF LOG-DOMAIN FILTERS USING THE E-CELL APPROACH

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A current goal in electronic system design is to develop low-voltage, low-power, low-cost, small-size, and high-dynamic range circuits. Analog filtering is a key signal processing application, and filtering approaches have been developed to fulfill the concurrent requirements of electronic systems. Log-domain filtering is a useful filtering approach, which exploits the nonlinear exponential relation between the current and voltage in the bipolar junction transistor (BJT) or the metal-oxide-semiconductor (MOS) field-effect transistor (FET) in the subthreshold region. Log-domain filtering provides electronically tunable, low-voltage, low-power, continuous-time current-mode, externally linear, and internally nonlinear filters. Methodologies for designing log-domain filters have been developed, and many transistor-level circuits have been designed. However, there has been little exploration of their internal operation.

In this dissertation, the nonlinear internal operation of log-domain filters is explored theoretically and systematically, with single-ended and differential log-domain filters designed by interconnecting the basic building blocks E cells. Large-signal analysis of log-domain filters conforms with the small-signal analysis of the current-mode transconductance-C (G_m-C) equivalent circuit at the operating point. Methods for adding common-mode feedback (CMFB) circuits to differential log-domain filters without degrading external linearity are presented. Simple but practical CMFB circuits are demonstrated. The CMFB allows derivation of closed-form expressions for the nonlinear internal signals. Differential second-order log-domain filters with CMFB circuits are built in the MOSIS 1.5 μm AMI ABN complementary MOS (CMOS) process. The theoretical analyses are supported by HSPICE simulations and experimental measurements. Finally, a design methodology based on E cells is generalized for implementing higher-order log-domain filters, presenting a systematic design procedure and possible ways to manipulate the circuits for a given transfer function.

CHAPTER 1
INTRODUCTION

1.1 Analog Filters

In analog filter design, filter specifications such as cutoff and center frequency, quality factor, passband gain, stopband gain, power dissipation, power supply voltage, distortion, and dynamic range characterize the filter transfer function. The specifications of linear filters should be constant and independent of signal levels. Nonlinearity is defined as how much those specifications vary from the constant values. In linear analog filters, the output signal frequency equals the input signal frequency. However, the output signal may contain other frequency components due to nonlinearity, which causes distortion in the filters. Total harmonic distortion (THD), a widely used measure of nonlinearity, is the ratio of the power of the harmonic frequency components to the power of the fundamental frequency component. Dynamic range is the ratio of the tolerable maximum signal (limited by nonlinearity) to the minimum signal (limited by noise) that can be processed. In practice, the tolerable maximum signal is the maximum signal amplitude that can be processed for a given THD, and the minimum signal is the minimum signal amplitude that can be processed for a given signal-to-noise ratio (SNR).

Among the filter specifications, cutoff and center frequency, quality factor, passband gain, and stopband gain may vary independently depending on random effect, such as process variation, power supply voltage variation, and temperature changes. Therefore, electronic tuning for those filter parameters is often required. The ability to adjust for variations of the parameters is tunability. For example, the cutoff frequency of a typical filter is proportional to the ratio of a transconductance to the capacitance, where the transconductance is the ratio of the output current to the input voltage of a transconductor (voltage controlled current source). If the transconductance and capacitance varied at the same rate, the cutoff frequency would not vary. However, if they vary at different rates, the cutoff frequency may vary from the expected value.

1.2 Linearity vs.Tunability

The resistor is a passive linear component, which produces a constant resistance for various applied signal levels. In integrated circuit (IC) technology, the resistance is determined by the conductivity and geometry of a layer. Thus once a resistor is fabricated, it is hard to tune the resistance electronically. Although a laser can be used to tune the fabricated resistor's geometry, laser tuning is expensive.

An example of an electronically tunable passive component is a varactor. The varactor is a voltage-controlled capacitor whose capacitance varies with the applied bias voltage. For small voltage signals, the varactor produces an approximately constant capacitance. However, for large voltage signals, the capacitance varies, causing nonlinearity. Therefore, the varactor is subject to tradeoff between tunability and linearity.

Passive LC filters use only passive components such as resistors, inductors and capacitors to set their time constants, thus the filters are not tunable. How-

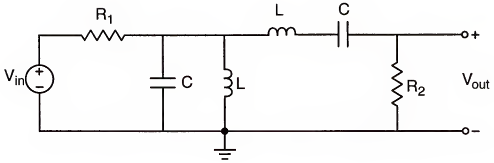


Figure 1.1 Fourth-order LC ladder bandpass filter.

ever, ladder structures, as shown in Figure 1.1, are used as the prototypes for active filters.

The tradeoffs between linearity and tunability are unavoidable in two-terminal passive components such as resistors, varactors, capacitors, and inductors. One more control terminal is needed to realize components which can be both linear and tunable. The transistor is a three-terminal component.

In a BJT transconductor, the exponential relation between the input voltage and the output current produces a nonlinear transconductance. Degeneration can make the transconductance inversely proportional to the added resistances, but loses tunability. MOSFETs in the triode region implement tunable resistors by using the gate voltages to vary the conductivity.

1.2.1 Active-RC Filter

Active-RC filters use resistors and capacitors with operational amplifiers to set time constants instead of inductors. Figure 1.2 shows an active-RC integrator, with the transfer function

$$\frac{V_{out}}{V_{in}} = -\frac{1}{sRC}. \tag{1.1}$$

The values of the passive components vary independently, so the filter time constant cannot be predicted accurately. Since the resistor and capacitor values are fixed, these time constant variations cannot be eliminated electronically.

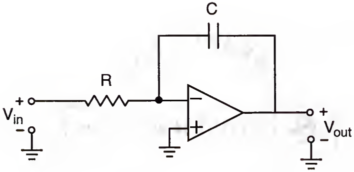


Figure 1.2 Active RC integrator with an op-amp.

1.2.2 MOSFET-C Filter

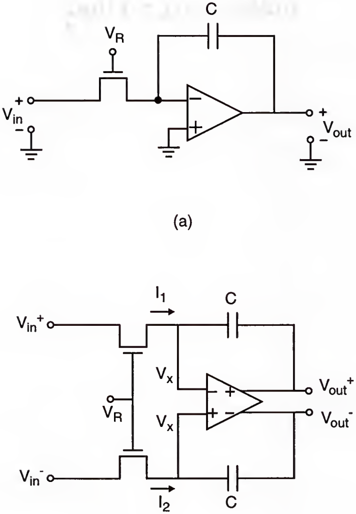
MOSFET-C filters replace the resistors in active-RC filters with MOSFETs operated in the triode region, as shown in Figure 1.3. In the triode region, the drain current can be approximated as

$$I_D = \frac{\mu C_{ox} W}{2} \frac{W}{L}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2]. \tag{1.2}$$

and the simulated resistor as

$$R \approx \frac{1}{\mu C_{ox}(W/L)(V_{GS} - V_{TH})}, \tag{1.3}$$

where V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, V_{TH} is the threshold voltage, W is the transistor channel width, L is the transistor channel length, C_{ox} is the gate capacitance per unit area, and μ is the mobility of carriers.



(a)

(b)

Figure 1.3 MOSFET-C integrator. (a) Single-ended integrator. (b) Differential integrator.

By varying the gate voltage V_R, MOSFETs simulate tunable resistors, resulting in electronic tunable filters. The MOSFET resistors are easily integrated in current processes. However, the MOSFET current includes terms with second-order dependence on voltage. The differential integrator shown in Figure 1.3 (b) eliminates the nonlinear second-order terms by subtracting two currents. The currents

$$I_1 = \frac{\mu C_{ox}}{2}\frac{W}{L}[2(V_R - V_x - V_{TH})(V_{in}^{+} - V_x) - (V_{in}^{+} - V_x)^2] \tag{1.4}$$

and

$$I_2 = \frac{\mu C_{ox}}{2}\frac{W}{L}[2(V_R - V_x - V_{TH})(V_{in}^{-} - V_x) - (V_{in}^{-} - V_x)^2]\ . \tag{1.5}$$

Note that the higher-order effects in the square law are not real. The subtraction of two currents

$$I_1 - I_2 = 2\mu C_{ox}\frac{W}{L}(V_R - V_{TH})V_{in}, \tag{1.6}$$

where $V_{in} = V_{in}^{+} - V_{in}^{-}$ cancels the nonlinear second-order terms. Then the resistor

$$R = \frac{1}{2\mu C_{ox}\frac{W}{L}(V_R - V_{TH})} \tag{1.7}$$

This illustrates a property of differential structures in that, assuming perfect subtraction, they eliminate even-order distortion, reducing overall distortion.

Both active-RC and MOSFET-C filters suffer from the frequency response limitations of operational amplifiers with their high loop gains. Also, distributed capacitances along “MOSFET resistor” degrade the frequency response.

1.2.3 Transconductance-C Filter

The transconductance-C (G_m-C) filter composed of transconductors and capacitors can avoid the frequency response limitations caused by high loop gain in closed-loop systems, since the transconductors are operated open-loop. The input and output signals of a transconductor are voltage and current signals, respectively, where the relation between the input and output is $I_{out} = G_m V_{in}$. G_m is an electronically variable transconductance. Figures 1.4 (a) and (b) show a single-ended G_m-C integrator and a differential G_m-C integrator with the output voltages

$$V_{out} = \frac{I_{out}}{sC} = \left(\frac{G_m}{sC}\right) V_{in}, \tag{1.8}$$

where s is the Laplace variable and unity-gain frequency $\omega_0 = G_m/C$. Figure 1.4 (c) shows a transistor-level differential transconductor using BJTs. The transconductance $G_m = g_m/(1 + g_m R)$, where $g_m = I_0/V_t$, I_0 is the bias current, and V_t is the thermal voltage kT/q. For T is the absolute temperature in kelvins (300 K at room temperature), V_t equals 26 mV, where k is Boltzmann's constant (1.38×10^{-23} joules/kelvin) and q is the magnitude of electronic charge (1.602×10^{-19} coulomb). If the unity-gain frequency changes due to the random variations, the unity-gain frequency can be tuned by adjusting I_0.

The degeneration lowers the transconductance G_m, increasing the input voltage swing. If $g_m R \gg 1$, G_m is linear but not tunable due to the passive resistor, else, G_m is tunable but becomes nonlinear due to the exponential relation of BJTs.

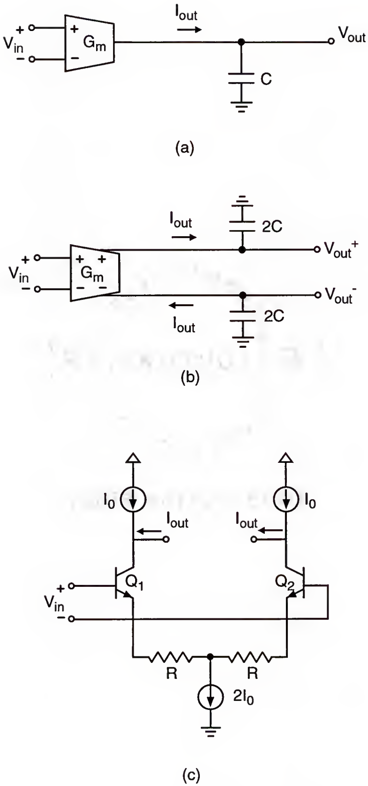


Figure 1.4 G_m-C filter. (a) Single-ended G_m-C integrator. (b) Differential G_m-C integrator. (c) Differential transconductor.

1.3 Log-Domain Filter

1.3.1 The Principle of Log-Domain Filtering

Continuous-time filters are useful for low-supply voltage, low-power consumption, high-dynamic range, high-frequency, and tunable applications such as anti-aliasing filter and phase equalization. Log-domain filtering is a variation of G_m-C filtering that presents a useful way to implement electronically tunable, integrated, continuous-time, current-mode filters. Instead of attempting to overcome the strong nonlinearity of the transistor, signals within the filter are allowed to be nonlinear, but the nonlinearities are arranged to cancel, preserving linearity of external transfer function.

The concept of log-domain filtering was proposed by Adams [Ada79], as shown in Figure 1.5. An applied input current signal I_{in} is converted to the input voltage V_{in} by an NPN transistor Q_1. The input voltage V_{in} is processed through a log-filter composed of a transistor Q_2, an integrating capacitor, and a current source I_0. The output voltage V_{out} is converted to the output current I_{out} by Q_3. The relations between the currents and voltages at the input and output are

$$V_{in} = V_D + V_t ln\left(\frac{I_{in}}{I_s}\right) \text{ and } \tag{1.9}$$

$$I_{out} = I_s exp\left(\frac{V_{out}}{V_t}\right), \tag{1.10}$$

where I_s is the BJT saturation current, and V_D is the voltage across a diode carrying current:

$$V_D = V_t ln\left(\frac{I_0}{I_s}\right). \tag{1.11}$$

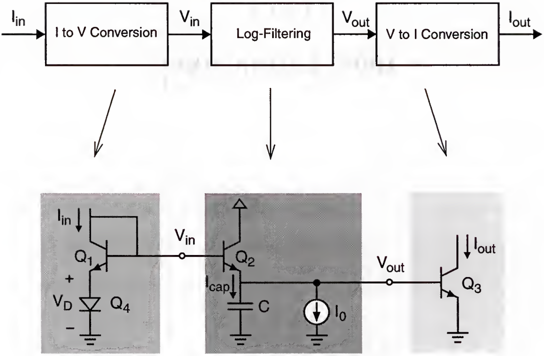


Figure 1.5 Principle of log-domain filtering.

Note that base currents of BJTs are neglected in (1.9) and (1.10). A nodal equation at V_{out} is

$$I_{cap} = C\frac{dV_{out}}{dt} = I_s exp\left(\frac{V_{in} - V_{out}}{V_t}\right) - I_0. \tag{1.12}$$

Substituting (1.9), (1.10), and (1.11) into (1.12) yields

$$C\frac{dV_{out}}{dt} = I_0\frac{I_{in}}{I_{out}} - I_0. \tag{1.13}$$

The chain-rule and manipulation of (1.10), (1.12), and (1.13) yield the linear differential equation

$$\frac{dI_{out}}{dt} = \frac{dI_{out}}{dV_{out}}\frac{dV_{out}}{dt} = \frac{I_{out}}{CV_t}\left(I_0\frac{I_{in}}{I_{out}} - I_0\right) = \frac{I_0}{CV_t}(I_{in} - I_{out}), \tag{1.14}$$

where the filter cutoff frequency $\omega_0 = I_0/CV_t$.

1.3.2 Translinear Circuits

Transistor-level log-domain circuits are composed of translinear loops formed by the base-emitter junctions of BJTs. The log-domain filter shown in Figure 1.5 can also be analyzed by the translinear principle. Gilbert proposed the translinear principle [Gil75] which is based on the relations

$$I_C = I_s exp\left(\frac{V_{BE}}{V_t}\right) \tag{1.15}$$

and

$$g_m = \frac{I_C}{V_t}, \tag{1.16}$$

where I_C is the collector current, V_{BE} is the base-emitter junction voltage, and g_m is the transconductance of BJTs. “Translinear” is a composite word reflecting that the transconductance of a BJT is linearly proportional to its collector current. A translinear loop is composed of even number of base-emitter junctions. Half of them is connected to raise the potential by V_{BE} and the rest half is connected to drop the potential in a translinear loop, regardless of the sequence of raising and dropping the potential.

The loop equation for the translinear loop composed of Q_4, Q_1, Q_2 and Q_3 in Figure 1.5 is

$$V_D + V_{BE1} = V_{BE2} + V_{BE3}, \tag{1.17}$$

where

$$V_{BE1} = V_t ln\left(\frac{I_{in}}{I_s}\right), \tag{1.18}$$

$$V_{BE2} = V_t ln\left(\frac{I_{cap} + I_0}{I_s}\right), \tag{1.19}$$

and

$$V_{BE3} = V_t ln\left(\frac{I_{out}}{I_s}\right). \tag{1.20}$$

Substituting (1.11), (1.18), (1.19), and (1.20) into (1.17) yields

$$I_0 I_{in} = (I_{cap} + I_0) I_{out}, \tag{1.21}$$

thus

$$I_{cap} = I_0 \frac{I_{in}}{I_{out}} - I_0. \tag{1.22}$$

Therefore, the translinear loop equation expressed by the summations of voltages in (1.17) is also expressed by the products of currents in (1.22) by the translinear principle.

1.3.3 Class A and Class AB Operations

In log-domain filters, an ac input signal current i_{in} is added to a dc bias current I_{bias}, resulting in the input current

$$I_{in} = i_{in} + I_{bias}. \tag{1.23}$$

The input current I_{in} must be positive to be processed within the filters, avoiding a BJT to be in cutoff mode. Only positive currents can be converted to voltages by the natural logarithmic expression shown in (1.9). Therefore, single-ended log-domain filters operate in Class A, where the applied signal currents must be less than dc bias currents. This Class A operation limits the maximum input signal current swing, restricting dynamic range.

However, Class AB operation allows input signal currents to be greater than bias currents. The input is split into two strictly positive currents whose difference equals the input signal current. The amplitudes of the positive currents can increase without bound depending on the input signal current, increasing dynamic range. Differential log-domain filters can operate in Class AB. The detailed operation of differential log-domain filters will be discussed in Chapter 4.

1.3.4 Implementations of Log-Domain Filters

After Adams' introduction of the log-filtering concept, Seevinck implemented the first log-domain integrator in 1990 [See90]. Frey designed the first log-domain filter in 1993 [Fre93], and several design and analysis methodologies for log-domain filters were proposed [Dra97, Dra99a, Elg97a, Fox98, Fre96b, Fre98, Mul97, Per95]. Tsividis defined log-domain filters as externally linear and internally nonlinear (ELIN) filters [Tsi97]. Many transistor-level circuits of single-ended log-domain filters have been presented [Dra99b, Dra00, Edw98, Elg97a, Elg99, Enz97, Fre96a, Fre96c, Fre96d, Fri96, Pun95, Pun96, Pun98, Tou94, Yan96]. Differential log-domain filters also have been presented [Elg97b, Elg98, Elg00a, Elg00b, Enz99, Fre99, Pun97, Pyt01, Wu98].

Most log-domain filters use BJTs. The MOSFET in the weak-inversion region also has an exponential relation between its gate-source voltage and its drain current. Thus, log-domain filters have also designed using MOSFETs in the weak-inversion region [Fri96, Geo01, Pyt99, Tou94].

1.4 Chapter Synopses

Chapter 2 will explain log-domain building blocks called E cells, categorize the E cells into E^+ cells and E^- cells, and demonstrate how to design first-order log-domain filters and integrators by interconnecting E cells and linear capacitors.

Next chapters involve new contribution of this dissertation to design and analysis of log-domain filters. Chapter 3 will demonstrate how to design single-ended second-order bandpass/lowpass log-domain filters, explore the nonlinear internal operation of second-order filters, and present how the nonlinear internal currents cause distortion, limiting dynamic range. HSPICE simulation results will demonstrate the distortion mechanism caused by the internal currents.

Chapter 4 will demonstrate how to design differential log-domain integrators, and how to add CMFB without degrading external linearity. Simple but practical CMFB circuits will be designed and added to differential second-order bandpass/lowpass log-domain filters. The CMFB circuits allow closed-form solutions for nonlinear differential output currents and decrease the peak internal currents, reducing THD. Differential second-order log-domain filters with and without CMFB circuits were be built in the MOSIS AMI ABN 1.5 μm CMOS process. Simulation and experimental results will be presented.

Chapter 5 will present nine ways to mix the CMFB circuits (geometric-mean CMFB and harmonic-mean CMFB) in differential second-order bandpass/lowpass filters. Idealized simulations will compare the peak amplitudes of the internal currents in the nine filters to find the combinations with the smallest currents. THD from the practical simulations will be presented.

Chapter 6 will generalize a design methodology based on E cells for implementing higher-order log-domain filters, presenting a systematic design procedure and possible ways to manipulate the circuits for a given transfer function.

Chapter 7 will conclude this dissertation, and propose future research of log-domain filters with CMFB.

CHAPTER 2
FIRST-ORDER LOG-DOMAIN FILTERS AND INTEGRATORS

2.1 Introduction

Several approaches have been developed for designing log-domain filters. Perry and Roberts proposed a design methodology based on LC ladder synthesis [Per95]. Yang, Enz, and Van Ruymbeke proposed a direct component-level mapping between linear-domain filters and log-domain filters [Yan96]. Frey proposed the time-varying nonlinear exponential mapping of the state variables to produce Kirchhoff's current law (KCL) equations for the synthesis of log-domain filters [Fre98, Fre00]. Drakakis, Payne, and Toumazou proposed the Bernoulli-cell approach [Dra99a]. An other useful design method is based on translinear building blocks called E cells [Fre96b]. The "E" comes from the fact that these cells exponentiate the difference of their two input voltages, producing an output current. The transistor-level circuits of E cells include an even number of base-emitter junctions, and can be connected to form translinear loops. E cell-based design is modular, since an E cell block can be replaced by many possible transistor-level circuits.

In this chapter, E cells will be defined and classified into E^+ cells and E^- cells. The small-signal equivalent circuit model of the E cells will be compared to that of a transconductor. A first-order log-domain filter and a log-domain integrator will be designed based on E cells. The E cell-based design approach arranges E cells so that their small-signal equivalent circuits match those of corresponding G_m-C filters.

2.2 Basic Building Blocks: E Cells

An E cell has two voltage inputs--a positive input V_+ and a negative input V_---an output, plus a reference current I_b. There are two types of E cells, E^+ cell and E^- cell. Both E^+ cell and E^- cell are classified as a sourcing E^+ cell or a sinking E^+ cell and a sinking E^- cell or a sourcing E^- cell by the direction of their output current.

2.2.1 Sourcing E+ Cells and Sinking E- Cells

The "sourcing E^+ cell" shown in Figure 2.1 (a) sources the positive output current,

$$I_{out} = I_b exp\left(\frac{V_+ - V_-}{V_t}\right). \tag{2.1}$$

The output node of the E^+ cell is often connected to the cell's inverting (V_-) input to form a negative feedback loop, as shown in Figure 2.1 (b), providing positive transconductance and positive output conductance equal to I_{out}/V_t.

Figure 2.1 (c) shows a possible transistor-level circuit of the sourcing E^+ cell. This circuit is composed of a diode-connected level-shifter and a voltage follower. The voltage follower, Q_2, performs the exponential function, producing I_{out}. The negative input and the output of this circuit is the same node, thus the negative feedback loop does not appear explicitly in Figure 2.1 (d).

The complementary cell type of a sourcing E^+ cell is a "sinking E^- cell." Figure 2.2 (a) shows a sinking E^- cell, which sinks the positive output current

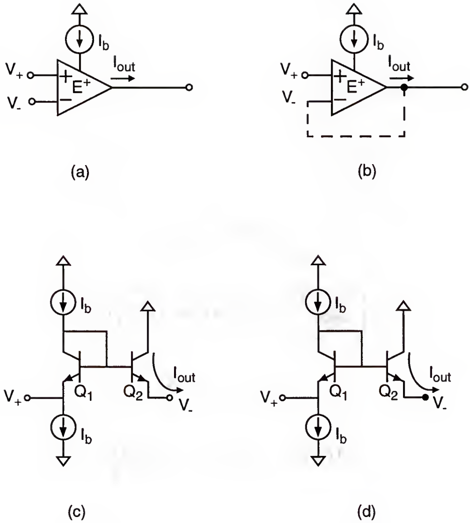


Figure 2.1 Sourcing E$^+$ cells. (a) An E$^+$ cell which sources $I_{out} = I_b exp[(V_+ - V_-)/V_t]$. (b) Input-output coupling of an E$^+$ cell, which provides a negative feedback loop. (c) A transistor-level implementation of E$^+$ cell shown in (a). (d) A transistor-level implementation of (b) is the same as (c).

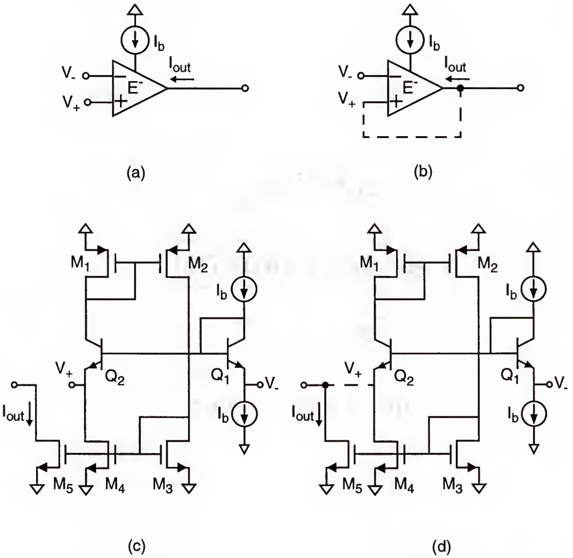


Figure 2.2 Sinking E^- cells. (a) An E^- cell which sinks the output current $I_{out} = I_b exp[(V_- - V_+)/V_t]$. (b) Input-output coupling of an E^- cell, which provides a positive feedback loop. (c) A transistor-level implementation of E^- cell shown in (a). (d) A transistor-level implementation of (b).

$$I_{out} = I_b exp\left(\frac{V_- - V_+}{V_t}\right). \tag{2.2}$$

Connecting the E- cell's V_+ terminal to its output node forms a positive feedback, as shown in Figure 2.2 (b), providing an inverted transconductance and a negative output conductance. Figure 2.2 (c) shows a transistor-level sinking E- cell [Fox97]. M_1 detects the collector current Q_2 and mirrors the current with M_2, and M_3, M_4, and M_5 provide a sign inversion of the current. Figure 2.2 (d) shows the positive feedback loop from V_+ to the output node of the E- cell circuit.

2.2.2 Sinking E+ Cells and Sourcing E- Cells

There is an alternate E cell definition in which E^+ cells sink the output current

$$I_{out} = I_b exp\left(\frac{V_- - V_+}{V_t}\right), \tag{2.3}$$

as shown in Figure 2.3 (a). Figure 2.3 (c) shows a transistor-level circuit of the sinking E- cell [Pun96]. The translinear loop composed of Q_1 and Q_2 gives a voltage-mode translinear equation

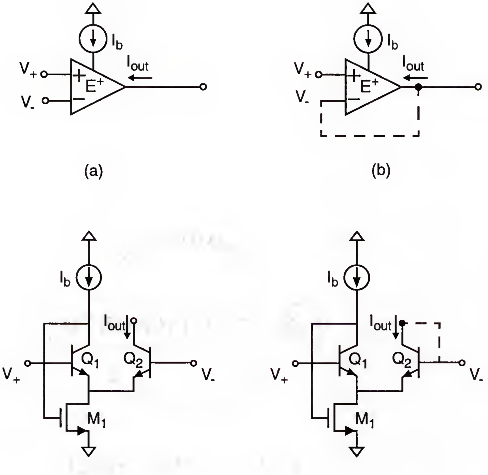
$$V_+ - V_{BE1} + V_{BE2} - V_- = 0, \tag{2.4}$$

where V_{BE1} and V_{BE2} are the base-emitter junction voltage of Q_1 and Q_2, respectively as

$$V_{BE1} = V_t ln\left(\frac{I_b}{I_s}\right) \tag{2.5}$$

and

$$V_{BE2} = V_t ln\left(\frac{I_{out}}{I_s}\right). \tag{2.6}$$



(a) (b) (c) (d)

Figure 2.3 Sinking E$^+$ cells. (a) An E$^+$ cell which sinks a current $I_{out} = I_b exp[(V_- - V_+)/V_t]$. (b) Input-output coupling of an E$^+$ cell, which provides a negative feedback loop. (c) A transistor-level implementation of E$^+$ cell shown in (a). (d) A transistor-level implementation of (b).

Substituting (2.5) and (2.6) into (2.4) gives

$$\frac{V_{-} - V_{+}}{V_T} = ln\left(\frac{I_{out}}{I_b}\right), \tag{2.7}$$

and thus

$$I_{out} = I_b exp\left(\frac{V_{-} - V_{+}}{V_t}\right). \tag{2.8}$$

The complementary cell type of an sinking E^+ cell is a "sourcing E^- cell," which sources the output current

$$I_{out} = I_b exp\left(\frac{V_{+} - V_{-}}{V_t}\right), \tag{2.9}$$

as shown in Figure 2.4 (a). Figure 2.4 (c) shows a transistor-level implementation of an sourcing E^- cell. The operation of the circuit is similar to the E^+ cell in Figure 2.3 (c) except that M_2 and M_3 are added to provide a signal inversion.

Four types of E cells have been explored. However, at the transistor level, there are only two types of E cells, since the same transistor-level circuit can be used for either a sourcing E^+ cell or a sourcing E^- cell, or for either a sinking E^+ cell or a sinking E^- cell, depending on the feedback connection.

2.2.3 Small-Signal Equivalent Circuit Models of E Cells

Figure 2.5 (a) shows a small-signal equivalent circuit model for an E^+ cell with a constant bias current at the zero signal operating point. This model represents the E^+ cell as a voltage-controlled current source, where the control voltage is the difference of v_+ and v_-. The input impedance is ideally infinite, typically, is the input impedance looking into the base of a BJT. The dotted line denotes the negative feedback loop from output node to v_- terminal. With the negative feedback, the model

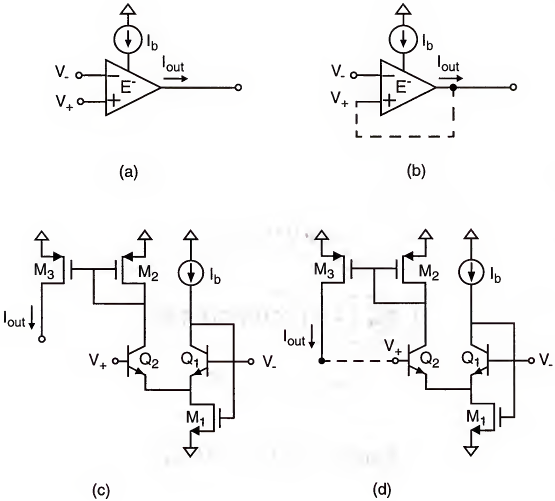
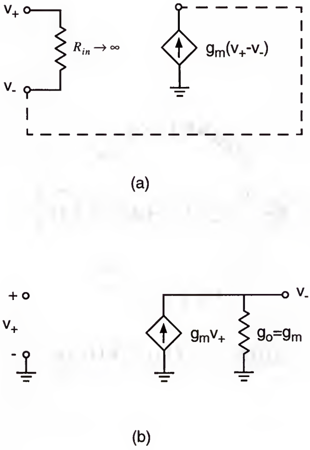


Figure 2.4 Sourcing E$^-$ cells. (a) An E$^-$ cell which sources a current $I_{out} = I_b exp[(V_+ - V_-)/V_t]$. (b) Input-output coupling of an E$^-$ cell, which provides a positive feedback loop. (c) A transistor-level implementation of E$^-$ cell shown in (a). (d) A transistor-level implementation of (b).

can be redrawn by with $g_m(v_+-v_-)$ replaced by $g_m v_I$ and an output conductance g_o, as shown in Figure 2.5 (b). Note that the output conductance g_o equals the transconductance g_m, whereas the output conductance of a transconductor is zero.



(a)

(b)

Figure 2.5 Small-signal equivalent circuit model of an E^+ cell with (a) $g_m(v_+-v_-)$, (b) $g_m v_+$ and g_m.

Figure 2.6 (a) and (b) show the corresponding equivalent circuit models of an E^- cell. The dotted line shows how a positive feedback loop can be formed from the output node to the v_+ terminal, resulting in a negative output conductance equal to $-g_m$. Note that both a sourcing E cell and a sinking E cell have the same small-signal equivalent circuit model.

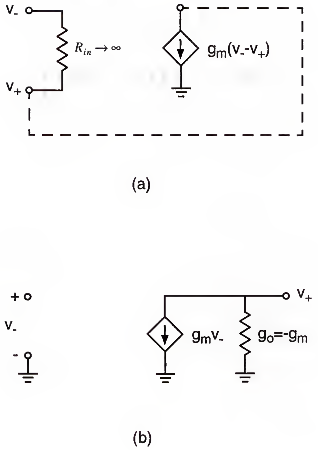


Figure 2.6 Small-signal equivalent circuit model of an E^- cell with (a) $g_m(v_- - v_+)$, (b) $g_m v_-$ and $-g_m$.

2.2.4 Alternative E-Cell Notation

In transistor-level circuits, Frey defined the E^+ cell's V_+ input as the voltage input which produces a noninverting output current, and the E^- cell's V_+ input as the voltage input which produces an inverting output current. However, in this dissertation, for E^+ cells and E^- cells, there is an even number of sign inversions (due to common-emitter or common-source stages) from the V_+ input to the output, and there is an odd number of sign inversions from the V_- input to the output. Figure

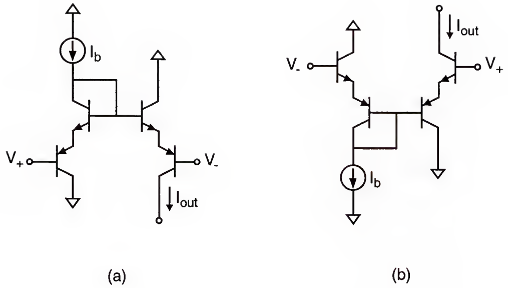


Figure 2.7 Transistor-level implementations of E cells with the input ports V_+ and V_- labelled by Frey. (a) E^+ cell. (b) E^- cell.

2.7 shows a sourcing E^+ cell and a sinking E^- cell labeled by Frey's definition. If the inputs are labeled depending on the number of signal inversions, the labels V_+ and V_- of the E^- cell shown in Figure 2.7 (b) are exchanged.

2.2.5 Example of E-Cell Circuits

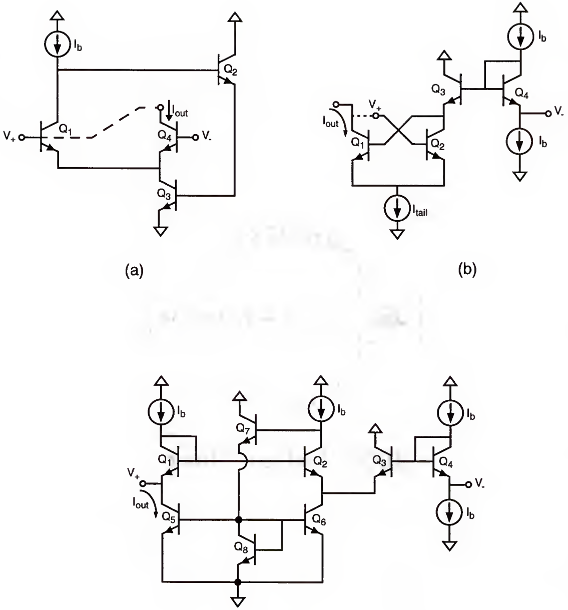
Several transistor-level implementations of E cells have been proposed. The E^- cell circuit proposed by Frey shown in Figure 2.8 (a) [Fre96d] is a sinking E^- cell. Q_2 and Q_3 force I_b to flow in Q_1, and the collector current of Q_4 is given by $I_0 exp((V_- - V_+)/V_t)$, which is I_{out}. Drakakis proposed the sinking E^- cell circuit [Dra97] shown in Figure 2.8 (b). The collector current of Q_1 is I_{out} of this E^- cell and represented as $I_{out} = I_{C3} = I_0 exp((V_- - V_+)/V_t)$. This E^- cell circuit will be discussed in detail in Chapter 3. El-Gamal proposed the E^- cell circuit [Elg99] shown in Figure 2.8 (c). The E^- cell composed of Q_1-Q_8 is a current-sinking cell that forms a positive feedback loop composed of Q_2, Q_1, Q_3, and Q_5 to produce a negative output conductance. The diode-connected transistor Q_8 can be replaced by a resistor or a current source for biasing Q_7.

The transistor-level E cells shown in Figures 2.3 (c) and 2.4 (c) require careful choice of the base bias voltage to prevent NPNs from operating in the saturation region. This constraint requires the consideration of the base voltage and W/L of M_1 simultaneously. If the W/L of M_1 is small, V_{GS} of M_1 increases, keeping the reverse bias between the collector and the base of Q_1. However, with small W/L, M_1 may enter the triode region on signal peaks, since the collector current of Q_2 can be much greater than the bias current during log-domain filter operation. (Details will be discussed in Chapter 3). On the other hand, using too large a W/L for M_1 decreases the V_{GS} of M_1 and forces Q_1 to operate in the saturation region since the collector voltage of Q_1 is set by the V_{GS} of M_1. Figure 2.9 (a) shows an additional NMOSFET, M_A, added in the feedback loop as a level shifter so that the collector voltage of Q_1 increases from $1V_{GS}$ in the previous case to $1V_{BE} + 1V_{GS}$. Figure 2.9 (b) is the corresponding enhanced E^- cell implementation. Note that the current source biasing of M_A could be replaced by a resistor, or a diode-connected FET [Kar00].

2.3 First-Order Log-Domain Filter Design

2.3.1 E Cell-Based Design

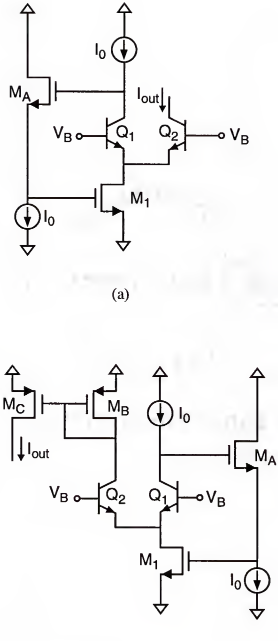
Figure 2.10 (a) shows a first-order log-domain filter composed of three E^+ cells. The input signal i_{in} is added to a bias current I_0 and applied to the current input terminal of $E_1{}^+$. The positive voltage input terminal V_+ is connected to a dc bias



(a) (b)

(c)

Figure 2.8 Examples of transistor-level E⁻ cells. (a) was proposed by Frey. (b) was proposed by Drakakis. (c) was proposed by El-Gamal.



(a)

(b)

Figure 2.9 Enhanced E cells. (a) E^+ cell. (b) E^- cell.

voltage source V_B. E_1^+ converts the input current I_{in} to a voltage V_{in}, E_2^+ and a capacitor at the output of E_2^+ process the voltage V_{in}, and E_3^+ converts the output voltage V_{out} to an output current I_{out}. Assuming that this filter uses sinking E^+ cells, then the output current of E_1^+ is given by

$$I_1 = I_{in} exp\left(\frac{V_{in} - V_B}{V_t}\right). \tag{2.10}$$

Some manipulation of (2.10) gives

$$V_{in} = V_B - V_t ln\left(\frac{I_{in}}{I_0}\right). \tag{2.11}$$

E_3^+ converts the output voltage V_{out} to the output current

$$I_{out} = I_0 exp\left(\frac{V_B - V_{out}}{V_t}\right), \tag{2.12}$$

thus

$$V_{out} = V_B - V_t ln\left(\frac{I_{out}}{I_0}\right). \tag{2.13}$$

The voltage-mode signal V_{in} is processed to produce V_{out} by E_2^+, capacitor C, and a bias current I_0 connected at the output of E_2^+. The output current of E_2^+, I_2, is given by

$$I_2 = I_0 exp\left(\frac{V_{out} - V_{in}}{V_t}\right). \tag{2.14}$$

Substituting (2.11) and (2.13) into (2.14) gives the current-mode equation

$$I_2 = I_0 \frac{I_{in}}{I_{out}}. \tag{2.15}$$

The nodal equation at the V_{out} node is

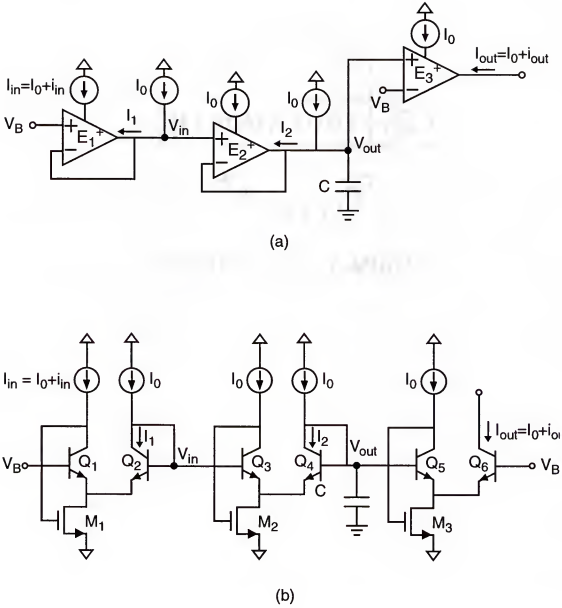


Figure 2.10 First-order log-domain filter using interconnected E cells. (a) Block diagram based on E cells. (b) Possible transistor-level implementation.

$$C\frac{dV_{out}}{dt} = I_0 - I_2 = I_0 - I_0\frac{I_{in}}{I_{out}}. \tag{2.16}$$

From (2.12),

$$\frac{dI_{out}}{dV_{out}} = \frac{di_{out}}{dV_{out}} = -\frac{I_{out}}{V_t}. \tag{2.17}$$

Using the chain rule and some manipulation of (2.16) and (2.17) gives a linear differential equation

$$\frac{di_{out}}{dt} = \frac{di_{out}}{dV_{out}}\frac{dV_{out}}{dt} = \frac{I_{out}}{CV_t}\left(I_0\frac{I_{in}}{I_{out}} - I_0\right) = \frac{I_0}{CV_t}(I_{in} - I_{out}) = \frac{I_0}{CV_t}(i_{in} - i_{out}). \tag{2.18}$$

Applying the Laplace transform to (2.18) gives the lowpass filter transfer function

$$H(s) = \frac{1}{\frac{s}{\omega_0} + 1}, \tag{2.19}$$

where $\omega_0 = I_0/CV_t$ is the cutoff frequency, which can be tuned through I_0 to overcome variations due to process or temperature. Figure 2.10 (b) shows a possible transistor-level implementation of the first-order log-domain filter based on interconnected E cells.

Instead of applying a current input as shown in Figure 2.10, a log-domain voltage input could be applied to the positive input port of E_1^+ with the dc bias voltage V_B. Note that, in the E cell-based designs, once the positive input V_+ of the input E^+ cell is connected to a dc bias voltage V_B, the internal nodes at the output of E cells have the same voltage as the dc voltage at the zero-signal operating point. Figure 2.11 shows a first-order log-domain filter based on Figure 2.10 (a) with the E^+ cell shown in Figure 2.1 (c). If the current densities of Q_1 and Q_2 at the zero-signal

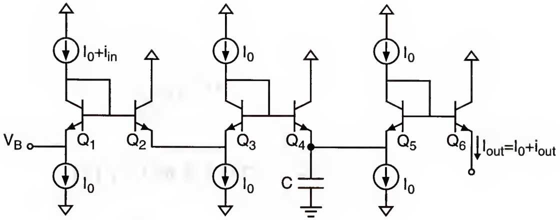


Figure 2.11 First-order log-domain filter implemented by the E^+ cell shown in Figure 2.1 (c).

operating point are equal, the emitter voltage of Q_2 is the same as V_B. Also, if the current densities of Q_3, Q_4, Q_5, and Q_6 are equal to that of Q_1, the emitter voltages of Q_4 and Q_6 are the same as V_B.

2.3.2 Simplification of E Cell-Based Filter

The first-order log-domain filter shown in Figure 2.10 (a) can be modified by merging E_1^+ and E_2^+, resulting in a simpler circuit, while keeping the external linearity and the transfer function. Figure 2.12 shows a modified first-order log-domain filter and its transistor-level implementation. E_1^+ performs current to voltage conversion and processes the converted voltage signal simultaneously. Thus V_{in} shown in Figure 2.10 (a) is no longer explicitly represented in Figure 2.12 (a).

2.3.3 Small-Signal Analysis

Conventional small-signal analysis also can be applied to log-domain filters and results in a linear transfer function at its zero signal operating point. Figure 2.13 shows a current-mode G_m-C small-signal equivalent circuit of the filter

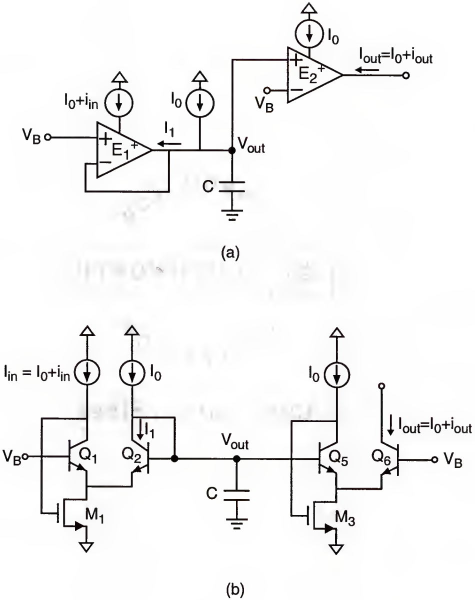


Figure 2.12 Modified first-order log-domain filter. (a) E cell-based filter. (b) Transistor-level implementation.

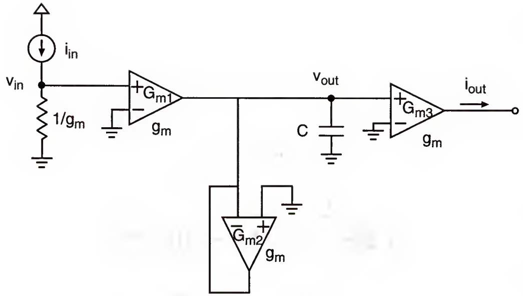


Figure 2.13 Current-mode G_m-C small-signal equivalent circuit of the first-order log-domain filter.

shown in Figure 2.10 (a). The resistor $1/g_m$ and the transconductor G_{m1} were converted from E_1^+, the negative feedback-connected G_{m2} from the bias current I_0, and G_{m3} from E_2^+. The transconductance of each transconductor is proportional to the bias current of the corresponding E cells.

Input signal current i_{in} is converted to v_{in} by

$$i_{in} = g_m v_{in}, \tag{2.20}$$

where g_m is the transconductance of a transconductor biased at I_0. At the output stage, i_{out} is given by

$$i_{out} = g_m v_{out} \tag{2.21}$$

and a nodal equation at v_{out} gives

$$g_m v_{in} = (g_m + sC) v_{out}. \tag{2.22}$$

From (2.20), (2.21), and (2.22)

$$\frac{i_{out}}{i_{in}} = \frac{1}{\frac{s}{\omega_0} + 1}, \tag{2.23}$$

where the cutoff frequency $\omega_0 = g_m/C = I_0/CV_t$.

2.4 Log-Domain Integrator Design

To convert the first-order log-domain filter from shown in Figure 2.12 to a log-domain undamped integrator, the positive output conductance of E_1^+ must be canceled. If the output of a negative-feedback-connected E^+ cell is connected to the output of a positive-feedback-connected E^- cell, the negative output conductance of the E^- cell cancels the positive output conductance of the E^+ cell when both the E^+ cell and E^- cell are equally biased and all signals are zero. Figure 2.14 shows a log-domain integrator with a zero net output conductance at V_{out}.

Figure 2.14 shows a log-domain integrator based on the interconnection of an E^+ cell and an E^- cell. Large-signal analyses give

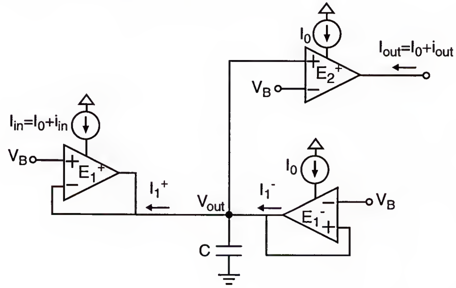


Figure 2.14 Log-domain integrator with a current input I_{in}.

$$I_1^{+} = I_{in} exp\left(\frac{V_{out} - V_B}{V_t}\right) = I_{in}\frac{I_0}{I_{out}}, \tag{2.24}$$

$$I_1^{-} = I_0 exp\left(\frac{V_{out} - V_B}{V_t}\right) = I_0\frac{I_0}{I_{out}}, \tag{2.25}$$

$$\text{where } I_{out} = I_0 exp\left(\frac{V_B - V_{out}}{V_t}\right). \tag{2.26}$$

The current through the capacitor is

$$C\frac{dV_{out}}{dt} = I_1^{-} - I_1^{+} \tag{2.27}$$

The chain rule and (2.17) yield the linear differential equation of the integrator:

$$\frac{di_{out}}{dt} = \frac{di_{out}}{dV_{out}}\frac{dV_{out}}{dt} = \frac{I_{out}}{CV_t}\left(I_{in}\frac{I_0}{I_{out}} - I_0\frac{I_0}{I_{out}}\right) = \frac{I_0}{CV_t}(I_{in} - I_0) = \frac{I_0}{CV_t}i_{in}. \tag{2.28}$$

Taking the Laplace transform of (2.28) gives an integrator transfer function

$$H(s) = \frac{\omega_0}{s}, \tag{2.29}$$

with unity-gain frequency $\omega_0 = I_0/CV_t$.

2.5 Conclusions

The E cell was defined as a translinear basic building block for designing log-domain filters. The E cell-based design approach to implement first-order log-domain filters and log-domain integrators were demonstrated. The E cell-based design method allows a modular approach. Conventional small-signal analysis can be applied to log-domain filters at the operating point, allowing log-domain filters to be designed by analogy to G_m-C filters. A negative feedback-connected E^+ cell produces a positive output conductance, and a positive feedback-connected E^- cell produces a negative output conductance. Damping is provided by adding a dc current source in the log-domain filter design, while that is provided by a resistance in the G_m-C filter design.

CHAPTER 3
SINGLE-ENDED SECOND-ORDER LOG-DOMAIN FILTERS

3.1 Introduction

Few design-oriented criteria have been presented for choosing device geometries to meet specified criteria, and little has been explored how to choose among transistor-level E-cell circuits. Although the input and output signal currents of log-domain filters are externally linear, their internal currents are nonlinear. The nonlinear internal currents can be extremely large, causing distortion unless the circuits and the transistor geometries can accommodate the huge currents.

Single-ended log-domain filter circuits operate Class A. However, the amplitudes of nonlinear internal currents can be much greater than the bias currents and can be infinite when the modulation index approaches unity. The peak amplitude of the internal currents can be estimated by simple mathematical expressions, and these estimates can be used for selecting transistor geometries and for choosing E-cell circuit topologies [Fox99a, Fox01b].

In practical applications, the large internal currents can affect the circuit performance in various ways. For example, the currents may overload the transistors in log-domain filters, causing distortion. To explore the effects of the nonlinear internal currents, the same single-ended second-order log-domain filter will be implemented using several transistor-level E cell circuits. HSPICE simulations will show the limitations caused by the large internal currents and demonstrate consistency with the mathematical expressions.

3.2 Design of Single-Ended Second-Order Filter

Figure 3.1 shows a single-ended second-order bandpass/lowpass log-domain filter based on interconnected E cells [Fox97]. E_1^+ converts the input current to voltage. E_3^+ and E_4^+ convert the bandpass and lowpass output voltages to the output currents. Damping is provided by the dc current source I_0/Q and the difference of the bias currents of E_1^+ and E_1^-.

A current-mode G_m-C small-signal equivalent circuit of the second-order log-domain filter in Figure 3.1 is shown in Figure 3.2. Transconductors G_{m1} and G_{m2} were converted from E_1^+, the negative feedback-connected G_{m3} from the bias current I_0/Q, G_{m4} from E_2^+, G_{m5} from E_1^-, G_{m6} from E_4^+ and G_{m7} from E_3^+. The transconductances of each transconductor are proportional to the bias currents of the corresponding E cells at the zero signal operating point.

Small-signal analysis at the input of the equivalent circuit gives

$$i_{in} = g_m\left(1 + \frac{1}{Q}\right)v_{in} \tag{3.1}$$

and the nodal equations at v_{oB} and v_{oL} are given by

$$g_m\left(1 + \frac{1}{Q}\right)v_{in} = \frac{g_m}{Q}v_{oB} + sC_1v_{oB} + g_mv_{oL} \tag{3.2}$$

and

$$g_mv_{oB} = sC_2v_{oL}, \tag{3.3}$$

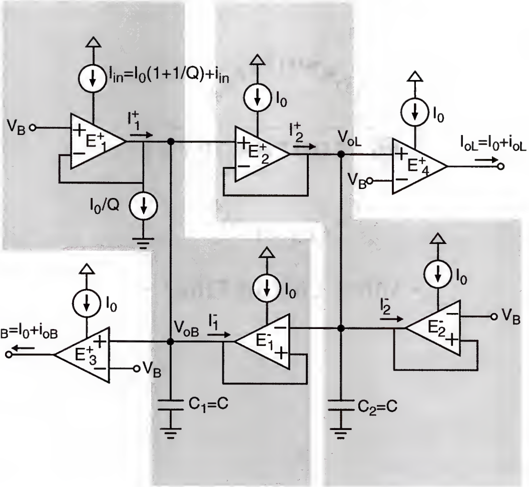


Figure 3.1 Single-ended second-order log-domain lowpass/bandpass filter.

respectively. The bandpass and lowpass output voltage-to-current conversions are given by

$$i_{oB} = g_m v_{oB} \tag{3.4}$$

and

$$i_{oL} = g_m v_{oL}. \tag{3.5}$$

Assuming $C_1 = C_2 = C$ and substituting v_{oL} from (3.3) into (3.2) gives

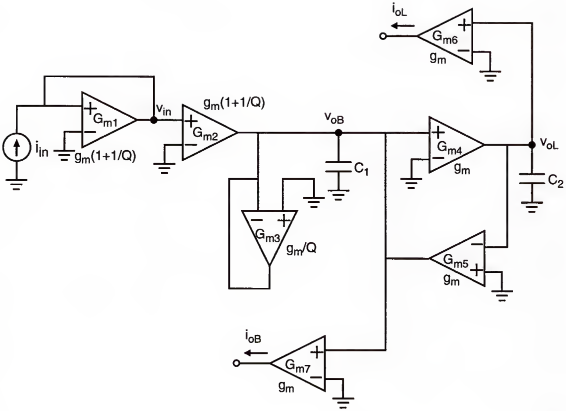


Figure 3.2 The current-mode G_m-C equivalent circuit of the second-order log-domain filter shown in Figure 3.1.

$$\frac{g_m}{sC}\left(1+\frac{1}{Q}\right)v_{in} = \left[\left(\frac{g_m}{sC}\right)^2+\left(\frac{g_m}{sC}\right)\frac{1}{Q}+1\right]v_{oB}. \tag{3.6}$$

Therefore,

$$\frac{v_{oB}}{v_{in}} = \frac{(1+1/Q)(s/\omega_0)}{(s/\omega_0)^2+(1/Q)(s/\omega_0)+1} \tag{3.7}$$

and from (3.3) and (3.7)

$$\frac{v_{oL}}{v_{in}} = \frac{v_{oB}}{v_{in}}\frac{g_m}{sC} = \frac{1+1/Q}{(s/\omega_0)^2+(1/Q)(s/\omega_0)+1} \tag{3.8}$$

(3.7) and (3.8) are voltage-mode transfer functions of bandpass and lowpass ports, respectively. The relations between output currents and voltages shown in equations (3.4) and (3.5) give the current-mode second-order bandpass and lowpass filter transfer functions as

$$\frac{i_{oB}}{i_{in}} = \frac{v_{oB}}{(1+1/Q)v_{in}} = \frac{(s/\omega_0)}{(s/\omega_0)^2+(1/Q)(s/\omega_0)+1} \tag{3.9}$$

and

$$\frac{i_{oL}}{i_{in}} = \frac{v_{oL}}{(1+1/Q)v_{in}} = \frac{1}{(s/\omega_0)^2+(1/Q)(s/\omega_0)+1}, \tag{3.10}$$

where $\omega_0 = g_m/C$ and $g_m = I_0/V_t$.

3.3 Internal Currents in Single-Ended Log-Domain Filters

In Figure 3.1, E_3^+ and E_4^+ are used for output conversion. Other E cells, E_1^+, E_2^+, E_1^-, and E_2^- are used for internal signal processing, producing internal nonlinear currents. Assume that sourcing E^+ cells and sinking E^- cells are used to build a second-order filter, as shown in Figure 3.1. From the translinear principle and the E cell's functions that produce the output currents, the nodal equation at node V_{oL} is

$$I_{C2} = I_2^+ - I_2^- = I_0\frac{I_{oB}(t)}{I_{oL}(t)} - I_0\frac{I_0}{I_{oL}(t)}, \tag{3.11}$$

where I_{C2} is the current in capacitor C_2. Obviously, if $I_{oL}(t)$ approaches zero while $I_{oB}(t)$ is nonzero, I_2^+ and I_2^- both increase without bound. Consider the case of a sinusoidal input at frequency ω such that

$$I_{oL}(t) = I_0[1+m\sin(\omega t)], \tag{3.12}$$

where m is the output modulation index defined as the ratio between peak output signal amplitude and a bias current I_0. From the bandpass filter transfer function (3.2),

$$I_{oB}(t) = I_0[1 + m(\omega/\omega_0)cos(\omega t)] . \tag{3.13}$$

For low frequencies ($\omega << \omega_0$), the bandpass output signal $i_{oB}(t)$ is attenuated by the filter, and $I_{oB}(t)$ is approximately constant at I_0. The lowpass filter passes the low-frequency input signal and the output signal $i_{oL}(t)$ appears without attenuation. Thus

$$I_2^+ = I_0\frac{I_{oB}(t)}{I_{oL}(t)} = I_0\frac{I_0}{I_0[1 + m sin(\omega t)]} = \frac{I_0}{1 + m sin(\omega t)} . \tag{3.14}$$

From (3.11) and (3.14), the maximum value of I_2^+ or I_2^- equals

$$I_{max} = \frac{I_0}{1 - m} \tag{3.15}$$

since the minimum of sin(ωt) is -1. For example, if an input signal of $m = 0.75$ is applied, then the maximum internal current $I_{max} = 4I_0$ from (3.15), and for $m = 0.95$, I_{max} rises to $20I_0$. As m goes to one, I_{max} goes to infinity. To operate without distortion, the filter must handle the large internal currents with ideal translinear behavior to avoid distortion of the output currents I_{oL} and I_{oB}.

The second-order filter shown in Figure 3.1 was designed using the sourcing E^+ cell and sinking E^- cell shown in Figures 2.1 (c) and 2.2 (c). Ideal models were used for all the transistors. The tuning current I_0 was set to 100 μA and C_1 and C_2 were set to 62.8 pF to give the filter cutoff/center frequency of 10 MHz. Filter Q was set to 0.707.

Figure 3.3 shows filter output currents I_{oB} and I_{oL} and two output currents of E_2^+ and E_2^-, which are the internal currents I_2^+ and I_2^- when a sinusoidal input signal with peak amplitude of 90 μA and frequency of 10 kHz was applied. Simulation results show that the lowpass output signal I_{oL} contains the dc bias current I_0 and the signal current i_{oL} and that the bandpass output signal I_{oB} contains only the bias current I_0 since the signal current i_{oB} was attenuated completely by the bandpass filter. The peak value of internal currents, I_2^+ and I_2^-, is 1000 μA, as predicted from (3.15) when $m = 0.9$.

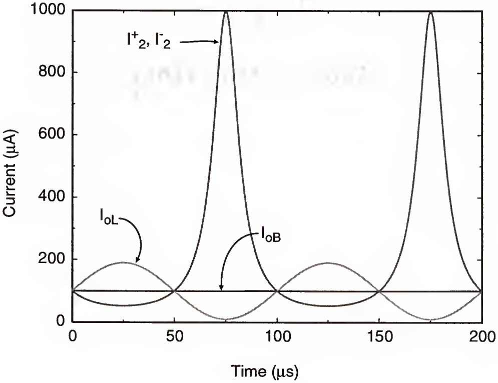


Figure 3.3 Simulated output and internal currents of a second-order filter implemented by the E cells shown in Figures 2.1 and 2.2 when the frequency of the applied input current is 500 Hz.

The current in C_1 is the difference of the internal output currents of E_1^+ and E_1^-:

$$I_{C1} = I_1^+ - I_1^- - I_0/Q, \tag{3.16}$$

where

$$I_1^+ = \left[I_0\left(1 + \frac{1}{Q}\right) + i_{in}\right]\frac{I_0}{I_{oB}(t)} \tag{3.17}$$

and

$$I_1^- = I_0\frac{I_{oL}(t)}{I_{oB}(t)}. \tag{3.18}$$

Maximum values of I_1^+ and I_1^- occur when the frequency of the applied input signal is equal to the center frequency, where the signal swing of I_{oB} is greatest. The maximum values of $I^+{}_1$ and I_1^- are approximately

$$I_1^+ = I_0\left(1 + \frac{1}{Q} - \frac{m}{Q}\right)/(1 - m) \tag{3.19}$$

and

$$I_1^- = \left(\frac{m}{Q}\right)/(1 - m), \tag{3.20}$$

respectively.

Figure 3.4 shows the simulation results of the output currents I_{oL} and I_{oB} and the internal currents I_1^+ and I_1^- when a sinusoidal input signal whose frequency is equal to the filter cutoff/center frequency was applied. Since the filter gain at this frequency is $Q = 0.707$, the amplitude of the input signal was set to $0.9/Q = 1.27\ I_0$ to give $m = 0.9$ for both outputs. Simulation results show that the magnitudes of both I_{oB} and I_{oL} are 180 $\mu A_{p\text{-}p}$ and that I_{oB} and I_{oL} are 90° out of phase. The peak values of I_I^+ and I_I^- are $11.5I_0$ and $12.3I_0$, respectively, values which coincide with those predicted by (3.19) and (3.20).

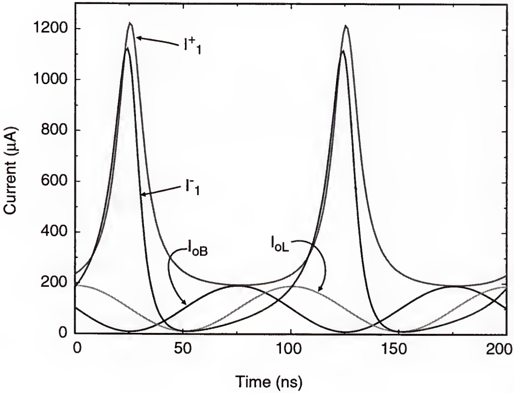


Figure 3.4 Simulated output and internal currents of a second-order filter implemented E cells shown in Figure 2.1 and Figure 2.2 were used to design the filter when the frequency of the applied input current is equal to the cutoff/center frequency.

3.3.1 Criteria for Transistor Geometries

It has been demonstrated that although the input and output signals of log-domain filters are linear, the internal currents are nonlinear, and the peak magnitude of the internal currents approaches infinity as the modulation index approaches unity, limiting dynamic range.

The following examples demonstrate the effects of internal currents on distortion of output currents. The single-ended second-order filter shown in Figure

3.1 was implemented with the E^+ cell in Figure 2.3 and the E^- cell in Figure 2.4. The filter specifications are cutoff/center frequency = 10 MHz, $Q = 0.707$, tuning current $I_0 = 100\ \mu A$, integrating capacitors $C_1 = C_2 = 62$ pF, and dc gain = 1. Ideal models were used for all transistors except for the PMOS current mirrors, which were designed with W/L = 96 μm/2.4 μm (AD = AS = $384(\mu m)^2$) so that the mirrors go into triode operation when the drain current of the p-channel MOS (PMOS) FET in E_2^- is greater than 338 μA, corresponding to a lowpass modulation index just over 0.7. The PMOS FET drain current corresponds to an internal current I_2^- and the peak magnitude of I_2^- equals that of I_2^+ in Figure 3.1.

From (3.15), when m equals 0.7, the predicted maximum of I_2^+ or I_2^- is $I_{2peak}^- = I_{2peak}^+ = 100\ \mu A/(1-0.7) = 333\ \mu A$. This means the PMOS FETs can accommodate the peak current and operate in saturation region. Thus the peak internal current does not cause distortion. However, when m equals 0.8, the predicted I_{2peak}^- is 500 μA, but the simulation result presented in Figure 3.5 shows the peak internal current is limited to well below 500 μA. This internal current waveform was distorted by the improper region operation of PMOS FETs in E_2^-. The distortion of the internal current causes distortion of the lowpass output current I_{oL}, resulting in nonlinear output current. THD simulations of the lowpass output current were performed using HSPICE. The THD simulations verify that unless the transistor geometries can accommodate peak internal currents, severe distortion is caused in the output signal, and also confirm (3.15). Figure 3.6 shows the THD levels from the HSPICE simulations and that THD in these idealized simulations is negligible for m

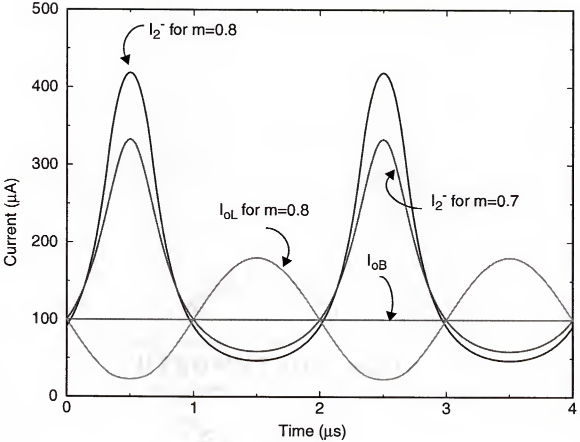


Figure 3.5 Currents in second-order filter using E cells shown in Figures 2.3 and 2.4. The input frequency in the simulations was well below the filter cutoff.

up to 0.7, but increases rapidly for *m* greater than 0.7 when the peak internal current I_2^- larger than the maximum current the PMOS FETs can handle, which is 333 μA.

To demonstrate the filter functionality, the frequency response is shown in Figure 3.7, where the cutoff/center frequency is 10 MHz and Q is set to 0.707, as predicted. The filter Q was set to 0.707, thus the magnitudes of the lowpass and the bandpass outputs are the same at the cutoff/center frequency.

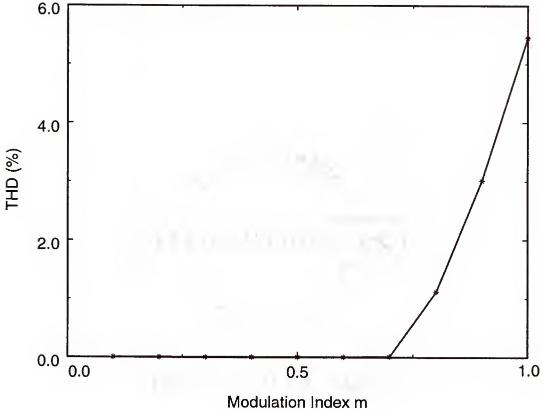


Figure 3.6 Distortion in second-order filter using E cells as in Figure 2.3 and Figure 2.4, reflecting increasing distortion of the lowpass output signal as PMOS FET M_2 in Figure 2.4 is over-driven.

3.3.2 Effects of Limited E- Cell Output Current

The sinking E^- cell shown in Figure 3.8 was proposed by Drakakis [Dra97, Dra98]. The base-emitter junctions of Q_3, Q_4, Q_5, and Q_6 form a translinear loop. The voltage-mode translinear loop equation is

$$V_- - V_+ = -V_{BE4} + V_{BE3} + V_{BE5} - V_{BE6}, \tag{3.21}$$

where V_{BE4}, V_{BE3}, V_{BE5}, and V_{BE6} are base-emitter junction voltages of Q_4, Q_3, Q_5, and Q_6, respectively. Assuming the transistors operate ideally, using the translinear principle, (3.21) is converted to a current-mode equation

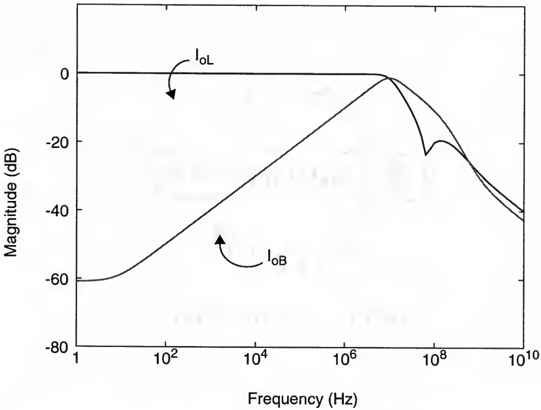


Figure 3.7 Simulated frequency response of a single-ended second-order log-domain filter based on E cells shown in Figure 2.3 and Figure 2.4.

$$I_{C3} = I_{C6}\frac{I_{C4}}{I_{C5}}exp\left(\frac{V_- - V_+}{V_t}\right), \tag{3.22}$$

where I_{C3}, I_{C4}, I_{C5}, and I_{C6} are the collector currents of Q_3, Q_4, Q_5, and Q_6, respectively. Since $I_{out} = I_{C3}$ and $I_{C4} = I_{C5}$,

$$I_{out} = I_{C3} = I_{C6}exp\left(\frac{V_- - V_+}{V_t}\right) = I_0 exp\left(\frac{V_- - V_+}{V_t}\right), \tag{3.23}$$

where $I_{C6} = I_0$. From (3.23), I_{out} is independent of the additional standby current source I_{tail}; however, the equation is only valid as long as

$$I_{C4} = I_{C5} = I_{tail} - I_{out} > 0, \tag{3.24}$$

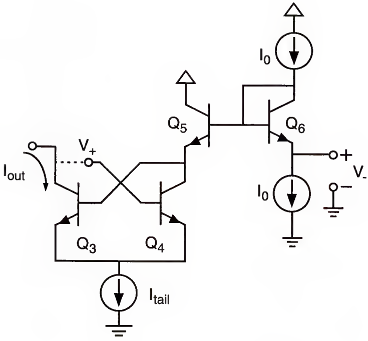


Figure 3.8 E$^-$ cell circuit from [Dra97]. Output current in this cell is limited by I_{tail}.

limiting the available output current from the E$^-$ cell.

A second-order log-domain filter was implemented based on Figure 3.1 with E$^+$ cells shown in Figure 2.3 and E$^-$ cells shown in Figure 3.8. Filter specifications are the same as the previous case: cutoff/center frequency = 10 MHz, $I_0 = 100\ \mu A$, $Q = 0.707$, and dc gain = 1. Figure 3.9 shows the filter functionality at both lowpass and bandpass output ports. The cutoff/center frequency is 10 MHz, and the same magnitude of lowpass and bandpass outputs at the cutoff/center frequency verifies Q equals 0.707.

From the filter structure shown in Figure 3.1, I_2^- is the output current of an E$^-$ cell, so I_{out} in Figure 3.8 corresponds to I_2^- in Figure 3.1 when the E$^-$ cell is

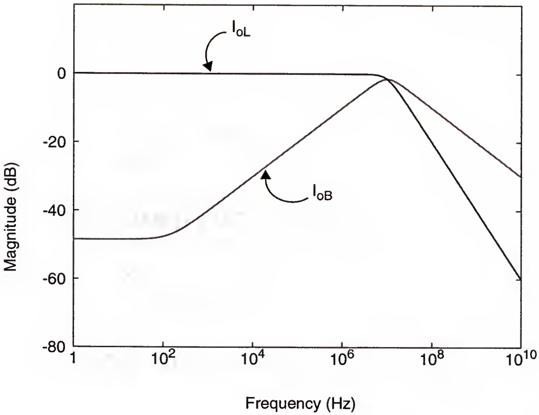


Figure 3.9 Simulated frequency response of a single-ended second-order log-domain filter composed of E^+ cells shown in Figure 2.1 (c) and E^- cells shown in Figure 3.8.

interconnected to implement a second-order log-domain filter. Note that I_{out} must be less than I_{tail} to keep I_{C4} and I_{C5} positive. Combining (3.11) and (3.24) gives

$$I_{tail} - I_{out} = I_{tail} - I_2^- = I_{tail} - I_0 \frac{I_0}{I_{oL}(t)} > 0 . \tag{3.25}$$

For the E^- cell to handle the maximum internal current derived in (3.15), I_{tail} must satisfy

$$I_{tail} > \frac{I_0}{1 - m} . \tag{3.26}$$

Thus the standby value of the I_{tail} must be greater than the maximum currents predicted in (3.15) to avoid clipping of the E cell currents. This would greatly increase the standby current requirements of filters using this E^- cell circuit.

Figure 3.10 shows the peak-to-peak lowpass output amplitude versus modulation index when very low frequency signals were applied. The filter was simulated when I_{tail} equals $2I_0$, $3I_0$, and $5I_0$, respectively. As the value of I_{tail} increases, larger signals can be processed without distortion. When I_{tail} was set to $5I_0$, the compression of the output signal starts when m equals 0.8, and when I_{tail} was set to $2I_0$, the compression starts when m equals 0.5 as it is predicted by (3.26).

Figure 3.11 shows the waveforms of the output currents and an internal current from the simulation when an input signal whose $m = 0.9$ and $\omega << \omega_0$ was applied and I_{tail} was set to $I_{tail} = 5I_0 = 500\ \mu A$. As predicted, the internal currents are larger than I_{tail} and have been clipped at 500 μA, since I_{tail} was set to 500 μA. The clipping of the internal currents causes significant distortion on the lowpass and bandpass output currents, I_{oL} and I_{oB}, simultaneously.

From (3.26), the maximum output modulation index for non-clipping of internal currents can be expressed in terms of I_{tail} and I_0 as

$$m_{max} = 1 - \frac{I_0}{I_{tail}}. \tag{3.27}$$

Figure 3.12 shows the resulting modulation index for 1% THD from HSPICE simulations for various I_{tail} and the maximum output modulation index calculated by equation (3.27). The modulation indices from the simulations and equation (3.27)

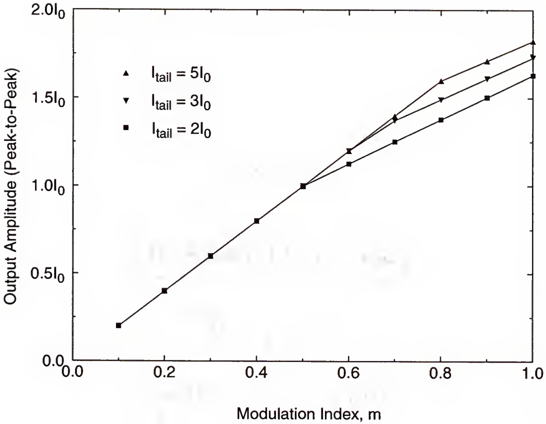


Figure 3.10 Peak-to-peak amplitudes of lowpass output currents versus modulation indices when the values of I_{tail} were set to $2I_0$, $3I_0$, and $5I_0$, respectively.

are consistent and thus show that the onset of distortion in this circuit can be predicted fairly accurately using equation (3.27).

3.4 Conclusions

In the analysis of single-ended second-order log-domain filters to determine input-output transfer functions, the internal currents supplied by the E cells are usually eliminated algebraically. However, these currents are nonlinear and can be much greater than the bias current in even Class A circuits. Simple mathematical expressions have been derived to predict the peak internal currents in the E cell-

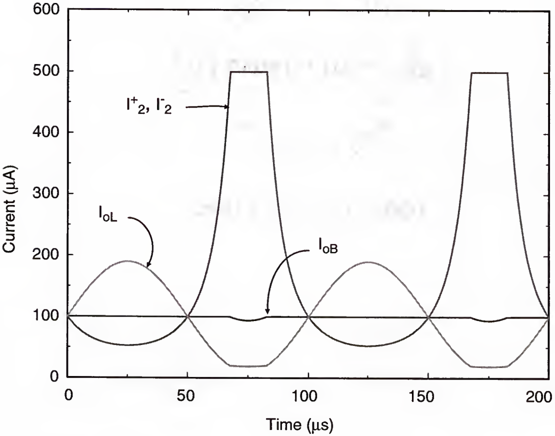


Figure 3.11 Simulation results analogous to those in Figure 3.3, except that the E$^-$ cells have been replaced with those from Figure 3.8, with I_{tail} set to $5I_0$ = 500 μA. The limited currents cause clipping of both the internal currents and the output currents.

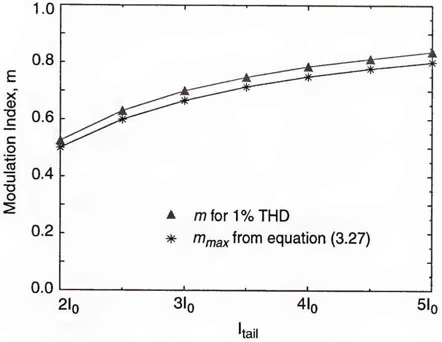


Figure 3.12 The modulation index at which low-frequency 1% THD occurs is consistent with equation (3.27) when E cell currents are limited by I_{tail}.

based single-ended second-order log-domain filter. The peak internal current should be considered in choosing E cells and transistor geometries in practical circuit designs.

CHAPTER 4
DIFFERENTIAL LOG-DOMAIN FILTERS

4.1 Introduction

Differential log-domain filters are designed to operate Class AB, extending dynamic range [Elg97b, Elg98, Elg00a, Elg00b, Enz99, Fre94, Fre99, Pun96, Pun97, Pyt01, Yan96]. In differential operation, an applied input current signal is split into a pair of positive currents whose difference equals the input signal. Typically, the product of the differential currents is forced to equal a constant [Dij98, Fre94, Pyt01], but other relationships are possible [Mul98, See88b].

A differential log-domain integrator, based on crossed-coupled E^- cells, was proposed [See90]. Differential log-domain filters were designed using the differential integrators [Elg98, Enz99, Fre99, Yan96]. However, one complication in the design of differential log-domain filters is that in general there are no closed-form solutions for the nonlinear signals within the filters. This makes it harder to select transistor geometries since it is not easy to predict peak currents for a given signal level.

This chapter will demonstrate how to add CMFB circuits to a differential second-order log-domain bandpass/lowpass filter without degrading the external linearity. Practical but simple CMFB circuits will be designed. The CMFB circuits allow closed-form solutions for nonlinear differential output currents, and decrease the peak internal currents, reducing THD. Simulation and experimental results will verify that the CMFB circuits allow increased signal swing of the log-domain filters, reducing distortion and increasing the dynamic range.

4.2 Differential Signal Processing

For differential log-domain filters, an applied input current i_{in} is split into the difference of a pair of strictly positive currents satisfying the differential-mode equation

$$i_{in} = I_{i1} - I_{i2} \tag{4.1}$$

and a common-mode equation, typically

$$I_{i1} I_{i2} = I_{Ref}^{2}, \tag{4.2}$$

where I_{Ref} is some reference current. The geometric-mean of I_{i1} and I_{i2} equals a constant reference current I_{Ref}. I_{i1} and I_{i2}, or their logarithmic voltage equivalents, are then applied as inputs to a differential log-domain filter. Figure 4.1 shows an input current waveform with the frequency of 500 Hz and the differential input currents I_{i1} and I_{i2}. The differential input currents are always positive and are both equal to the dc bias current when no input current is applied, where the dc bias current is 15 μA in Figure 4.1. When a pair of differential input currents are applied to a differential log-domain filter, the filter produces a pair of differential output currents I_{o1} and I_{o2}. The linear output current

$$i_{out} = I_{o1} - I_{o2}. \tag{4.3}$$

Although the differential currents processed within the differential filter are nonlinear due to the geometric-mean operation shown in (4.2), the external input and output currents are linear since the nonlinearity is cancelled by subtracting a differential current from another differential pair current.

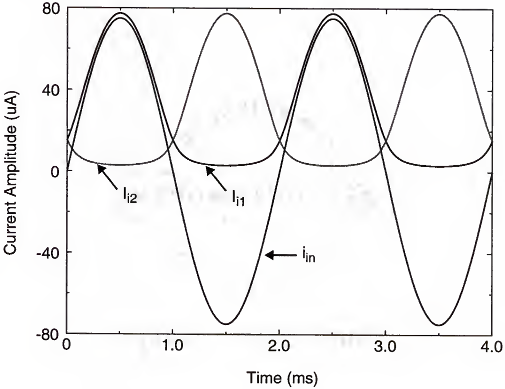


Figure 4.1 Input current I_{in} and its split differential currents I_{i1} and I_{i2}.

4.2.1 Current Splitter

To split an input current to differential currents, the subtraction and the geometric-mean operation represented in (4.1) and (4.2) are implemented by a current splitter. Figure 4.2 shows a simple geometric-mean current splitter [Fre96b]. This circuit implements (4.1) while producing output voltages V_1 and V_2 satisfying

$$V_1 + V_2 = V_{be1} + V_{be2} = 2V_D, \tag{4.4}$$

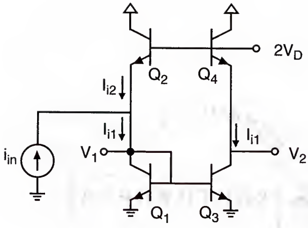


Figure 4.2 Geometric-mean current splitter.

where $V_D = V_t \, ln \, (I_0 / I_s)$ is the V_{BE} of an ideal transistor operated with collector current I_0. By the translinear principle, the voltage-mode translinear loop equation shown in (4.4) is converted to a current-mode translinear loop equation,

$$\sqrt{I_{i1} I_{i2}} = I_0, \tag{4.5}$$

so the geometric-mean of the two inputs I_{i1} and I_{i2} is fixed at a constant. From (4.1) and (4.5),

$$I_{i1} = \frac{\sqrt{i_{in}^2 + 4I_0^2} + i_{in}}{2} \tag{4.6}$$

and

$$I_{i2} = \frac{\sqrt{i_{in}^2 + 4I_0^2} - i_{in}}{2} \tag{4.7}$$

Also, currents I_{i1} and I_{i2} are

$$I_{i1} = I_0 exp\left(\frac{V_1 - V_D}{V_t}\right) \tag{4.8}$$

and

$$I_{i2} = I_0 exp\left(\frac{V_2 - V_D}{V_t}\right) = I_0 exp\left[\frac{-(V_1 - V_D)}{V_t}\right], \tag{4.9}$$

respectively, so that

$$i_{in} = I_0 exp\left(\frac{V_1 - V_D}{V_t}\right) - I_0 exp\left[\frac{-(V_1 - V_D)}{V_t}\right] = 2I_0 sinh\left(\frac{V_1 - V_D}{V_t}\right). \tag{4.10}$$

Therefore,

$$\frac{V_1 - V_D}{V_t} = asinh\left(\frac{i_{in}}{2I_0}\right) \tag{4.11}$$

Substituting (4.11) into (4.8) and (4.9) gives

$$I_{i1} = I_0 exp\left[asinh\left(\frac{i_{in}}{2I_0}\right)\right] \tag{4.12}$$

and

$$I_{i2} = I_0 exp\left[-asinh\left(\frac{i_{in}}{2I_0}\right)\right]. \tag{4.13}$$

However, the nonzero base currents of Q_1 and Q_3 in the current splitter causes inaccuracies, causing distortion. Figure 4.3 [Fox00] shows a modified current splitter. Instead of using the diode-connected Q_1 in Figure 4.2, the circuit has a negative feedback loop through Q_3, Q_4, Q_5, M_3, and M_2. Note that the diode connection of Q_3 is replaced by a source follower M_4 that supplies the base currents of Q_3 and Q_4 to compensate for errors due to finite β. A bias voltage V_B is applied to the base of Q_1, Q_2, and Q_5.

4.2.2 Input Signal Conditioner

The current splitter provides different signal paths for a pair of differential currents. Path mismatch may cause distortion when high-frequency signals are

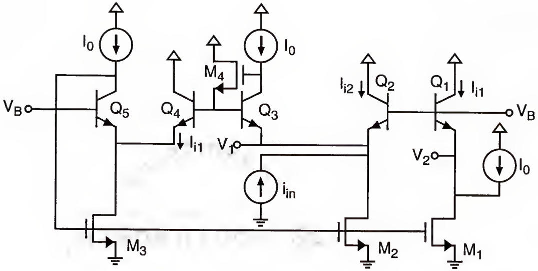


Figure 4.3 Modified geometric-mean current splitter for low-voltage operations.

applied. A possible way to provide a pair of symmetric signal paths for both differential currents is using a transformer and an input signal conditioner. The transformer converts an input signal current to a pair of positive currents. Figure 4.4 shows a input signal conditioner modified from the current splitter shown in Figure 4.3. The input signal source, i_{in}, shown in Figure 4.4 can be implemented by a current source and a transformer in practical applications. The collector currents of Q_{1A} and Q_{1B} are a pair of the input currents, and are applied to a differential filter.

4.3 Differential Log-Domain Integrator

Figure 4.5 shows a differential log-domain integrator based on cross-coupled E^- cells [Elg98, Enz99, Fox99b, Fre99, See90, Yan96]. The differential log-domain integrator is composed of E^+ cells (E_5^+ and E_6^+) terminated by capacitors, cross-coupled E^- cells (E_1^- and E_2^-), and two capacitors. The positive inputs of E_1^- and E_2^- are biased at V_B. The shaded area is the core of the differential integrator that

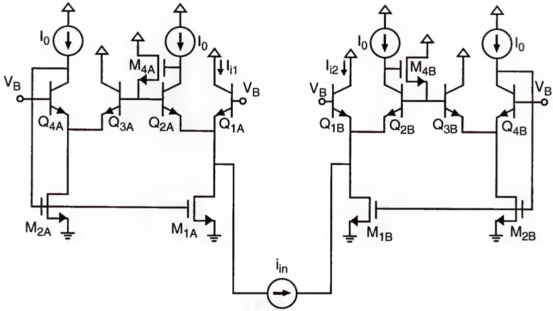


Figure 4.4 Input signal conditioner. The signal current source, i_{in}, is implemented by a current source and a transformer.

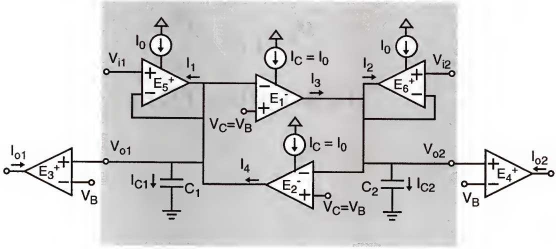


Figure 4.5 Differential integrator formed by cross-coupled E^- cells and E^+ cells terminated by capacitors.

operates on the log-domain input voltages V_{i1} and V_{i2} to produce output voltages V_{o1} and V_{o2}. All E cells of the core are biased equally at I_0. When a pair of differential input currents are applied, the currents are added to the reference input currents of E_5^+ and E_6^+. The output conversion E cells, E_3^+ and E_4^+, convert the output voltages V_{o1} and V_{o2} to the output currents I_{o1} and I_{o2}, respectively.

If the differential integrator is implemented with a sinking E^+ cell and a sourcing E^- cell, the differential output currents,

$$I_{o1} = I_0 exp[(V_B - V_{o1})/V_t] \text{ and } \tag{4.14}$$

$$I_{o2} = I_0 exp[(V_B - V_{o2})/V_t], \tag{4.15}$$

are produced by E_3^+ and E_4^+. The linear output current is

$$i_{out} = I_{o1} - I_{o2}. \tag{4.16}$$

If two additional conversion E^+ cells were added, the differential input currents I_{i1} and I_{i2} could be regenerated from V_{i1} and V_{i2} as

$$I_{i1} = I_0 exp[(V_B - V_{i1})/V_t] \text{ and } \tag{4.17}$$

$$I_{i2} = I_0 exp[(V_B - V_{i2})/V_t]. \tag{4.18}$$

Then, the linear input current

$$i_{in} = I_{i1} - I_{i2}, \tag{4.19}$$

could be regenerated by subtracting the output currents of two additional conversion E^+ cells.

Using the relations between the output current and the input voltages of the sinking E^- cell and the sourcing E^+ cell, and the translinear principle, the output currents of E_5^+, E_6^+, E_1^- and E_2^-, which are labeled I_1, I_2, I_3, and I_4, are

$$I_1 = I_0 exp\left(\frac{V_{o1} - V_{i1}}{V_t}\right) = I_0\frac{I_{i1}}{I_{o1}}, \tag{4.20}$$

$$I_2 = I_0 exp\left(\frac{V_{o2} - V_{i2}}{V_t}\right) = I_0\frac{I_{i2}}{I_{o2}}, \tag{4.21}$$

$$I_3 = I_0 exp\left(\frac{V_B - V_{o1}}{V_t}\right) = I_0\frac{I_{o1}}{I_0}, \tag{4.22}$$

and

$$I_4 = I_0 exp\left(\frac{V_B - V_{o2}}{V_t}\right) = I_0\frac{I_{o2}}{I_0}, \tag{4.23}$$

respectively. Therefore, the capacitor currents I_{C1} and I_{C2} can be expressed using (4.20), (4.21), (4.22), and (4.23) as

$$I_{C1} = I_4 - I_1 = I_{o2} - I_0\frac{I_{i1}}{I_{o1}} = C_1\frac{dV_{o1}}{dt} \tag{4.24}$$

and

$$I_{C2} = I_3 - I_2 = I_{o1} - I_0\frac{I_{i2}}{I_{o2}} = C_2\frac{dV_{o2}}{dt}. \tag{4.25}$$

Using (4.14), (4.15), (4.24), and (4.25), the circuit's nodal equations and the chain rule yield the differential equations

$$\frac{dI_{o1}}{dt} = \frac{dI_{o1}}{dV_{o1}}\frac{dV_{o1}}{dt} = \frac{I_{o1}}{V_tC}\left[I_0\frac{I_{i1}}{I_{o1}} - I_{o2}\right] = \frac{I_0}{V_tC}\left[I_{i1} - \frac{I_{o1}I_{o2}}{I_0}\right] \tag{4.26}$$

and

$$\frac{dI_{o2}}{dt} = \frac{dI_{o2}}{dV_{o2}}\frac{dV_{o2}}{dt} = \frac{I_{o2}}{V_tC}\left[I_0\frac{I_{i2}}{I_{o2}} - I_{o1}\right] = \frac{I_0}{V_tC}\left[I_{i2} - \frac{I_{o1}I_{o2}}{I_0}\right]. \tag{4.27}$$

The first terms in the brackets in (4.26) and (4.27) represent the E$^+$-cell output current, and the second term represents the E$^-$-cell output current. If I_{o1} and I_{o2} are subtracted, the nonlinear terms (the second terms in the brackets) cancel, yielding the equation of a linear current-mode integrator,

$$\frac{di_{out}}{dt} = \frac{d}{dt}(I_{o1} - I_{o2}) = \frac{I_0}{V_t C}[I_{i1} - I_{i2}] = \frac{I_0}{V_t C} i_{in}, \tag{4.28}$$

where $I_0/(V_t C)$ is the unity-gain frequency ω_0.

4.3.1 Small-Signal Analysis

In differential-mode small-signal analysis at the zero signal bias point, the negative output conductances of the E$^-$ cells cancel the positive output conductance of the E$^+$ cells at V_{o1} and V_{o2}, resulting in the zero net output conductances of an ideal differential log-domain integrator. However, in common-mode small-signal analysis, the cross-coupled E$^-$ cells provide positive damping. Figure 4.6 shows the common-mode equivalent of the cross-coupled E$^-$ cells. The negative inputs and the outputs of each E$^-$ cell are coupled, and the positive inputs of both E$^-$ cells are connected to V_B. The small-signal common-mode output conductance

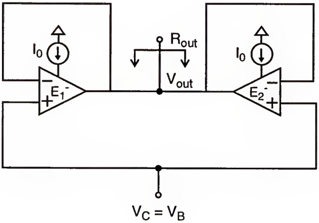


Figure 4.6 Common-mode equivalent of cross-coupled E$^-$ cells.

$$G_{CM} = \frac{1}{R_{out}} = \frac{1}{\frac{1}{g_{m0}} \| \frac{1}{g_{m0}}} = 2g_{m0}, \tag{4.29}$$

where $g_{m0} = I_0/V_t$ is the zero-signal transconductance for all the BJTs.

Figure 4.7 (a) shows a transistor-level differential log-domain integrator, implemented using the E^+ and E^- cells from Figures 2.3 (c) and 2.4 (c). Shading has been used to highlight E_5^+ and E_1^-. The level-shifters in E_3^+ and E_4^+ have been omitted since the level-shifters in E_1^- and E_2^- perform the same function. Therefore, the output conversion transistors Q_3 and Q_8 in E_3^+ and E_4^+ are connected to the level-shifters Q_2 - M_2 and Q_7 - M_8, respectively, where these level-shifters are in E_1^- and E_2^-. Bias voltage V_B is set to about 1 V, and V_C is set equal to V_B. V_D is the voltage across a diode carrying current I_0: $V_D = V_t\, ln(I_0/I_s)$. Figure 4.7 (b) shows the small-signal common-mode equivalent half-circuit. The Q_2 - M_2 buffer is represented as a unity-gain voltage-controlled voltage source. The current-mirror input MOSFETs M_3 and M_9 are in parallel for common-mode signals, so the signal path is shown passing from M_3 and M_4. The buffered common-mode signal v_{ocm} is amplified by Q_4 with common-base transconductance g_{m0}. The resulting current signal is mirrored by the unity-gain current-mirror, which is loaded by diode-connected Q_1, whose conductance is also g_{m0}. Thus the dc common-mode loop gain T_{CM} is verified to equal one, and the shunt feedback yields $G_{CM} = g_{m0}(1+T_{CM}) = 2g_{m0}$, as in (4.29).

4.3.2 Differential Second-Order Log-Domain Filter

Figure 4.8 shows how E cells can be interconnected to form a differential second-order lowpass/bandpass log-domain filter. This filter is composed of an input signal conditioner, damping E cells E_{D1}^+ and E_{D2}^+, and the differential inte-

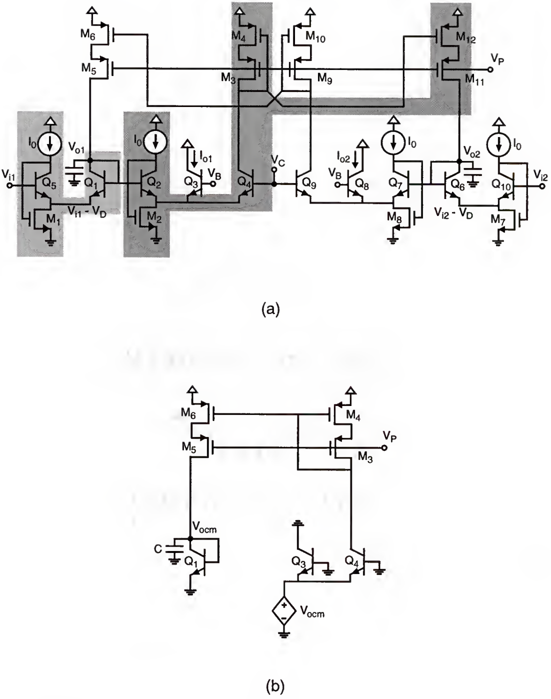


Figure 4.7 Differential log-domain integrator. (a) Integrator based on the circuit shown in Figures 2.3 and 2.4. (b) Small-signal common-mode equivalent circuit.

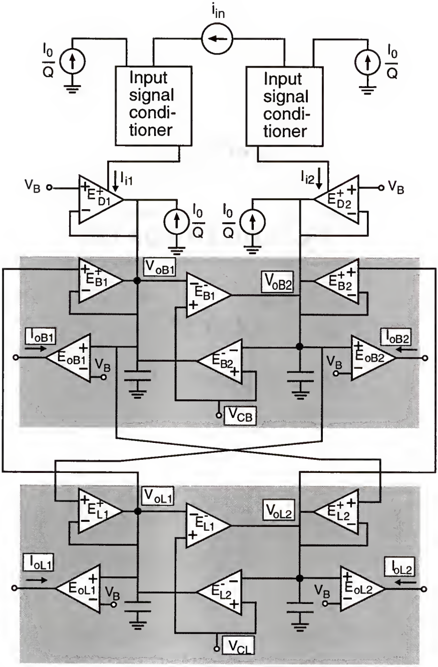


Figure 4.8 Differential second-order log-domain bandpass/lowpass filter.

grators. The core of the filter is a resonator based on a cross-coupled pair of log-domain integrators, forming a log-domain gyrator. All reference current inputs are set to the tuning current I_0 except for E_{D1}^+ and E_{D2}^+, whose reference current inputs are driven by the signal conditioner outputs. Damping is provided by the added dc current sources I_0/Q. Output currents can be derived using current subtractors implemented by PMOSFET current mirrors.

4.4 Common-Mode Feedback Circuits

4.4.1 Conditions for Adding CMFB

Examination of (4.26) and (4.27) shows that the nonlinear terms still cancel, and (4.28) still applies if these equations are replaced by the more general form

$$\frac{dI_{o1}}{dt} = \frac{I_{o1}}{V_t C}\left[I_0 \frac{I_{i1}}{I_{o1}} - f(1,2) I_{o2}\right] \tag{4.30}$$

and

$$\frac{dI_{o2}}{dt} = \frac{I_{o2}}{V_t C}\left[I_0 \frac{I_{i2}}{I_{o2}} - f(1,2) I_{o1}\right], \tag{4.31}$$

as long as the function f is a CM signal that operates on a signal pair symmetrically so that $f(1,2) = f(2,1)$. To keep the operating point (and thus the integrator's frequency response) unchanged, f must equal the reference current I_0 at the filter's zero-signal steady-state operating point. Any common-mode signal represented as a current can be applied to the I_C inputs of E_1^- and E_2^- in Figure 4.5, as long as I_C equals I_0 at the zero-signal operating point. Alternatively, a common-mode signal expressed as a voltage can be applied to the V_C ports in Figure 4.5 if the zero-signal value of V_C equals V_B. Thus we can use V_C or I_C as an input port for CMFB.

Figure 4.9 shows how voltage-mode CMFB can be applied to a differential second-order filter. This figure shows only the bandpass section. The CMFB circuit detects the bandpass output voltages V_{oB1} and V_{oB2}, processes the voltage signals, and provides the CM signal to the inputs of E_{B1}^- and E_{B2}^-. The detailed operation of several CMFB circuits [Fox01a] will be demonstrated in the following sections. CMFB can also be added at the lowpass section of the second-order filter.

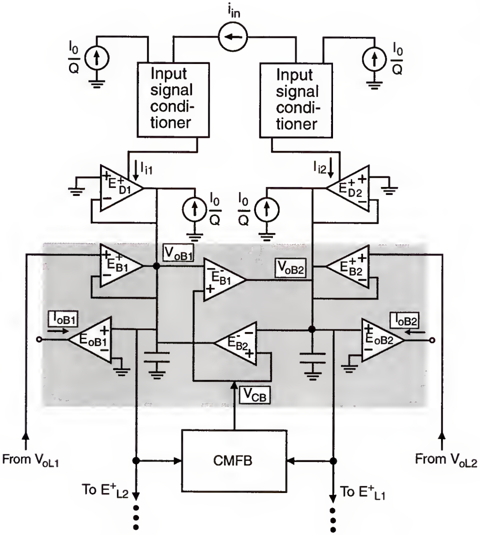


Figure 4.9 Differential second-order bandpass/lowpass filter with CMFB. Only the bandpass part is shown.

4.4.2 Arithmetic-Mean CMFB

One way to generate the CMFB is to sum the output currents and feed a resulting amplified voltage back to V_C, as shown in Figure 4.10. This circuit detects any difference between $I_{o1} + I_{o2}$ and $2I_0$, amplifies this error by a large loop gain, and feeds the result back through the V_C ports of the cross-coupled E$^-$ cells. The feedback forces the error to zero so that $I_{o1} + I_{o2} = 2I_0$. The output currents can be expressed in closed form as

$$I_{o1} = I_0 + \frac{i_{out}}{2} \text{ and} \tag{4.32}$$

$$I_{o2} = I_0 - \frac{i_{out}}{2}. \tag{4.33}$$

Since only positive values of the currents can be handled without clipping, Class AB operation is not possible with this circuit: the maximum differential signal swing is reduced to $2I_0$.

4.4.3 Geometric-Mean CMFB

Another CMFB alternative is to detect and amplify $(V_{o1} + V_{o2})/2 - V_B$, and let the feedback force that difference toward zero. This can be implemented using the circuit shown in Figure 4.11. Keeping the sum of V_{o1} and V_{o2} constant is equivalent to keeping the geometric-mean of I_{o1} and I_{o2} constant by the translinear principle. This leads to a set of closed-form solutions for the differential output currents. The closed-form solutions are

$$I_{o1} = \frac{\sqrt{i_{out}^2 + 4I_0^2} + i_{out}}{2} \tag{4.34}$$

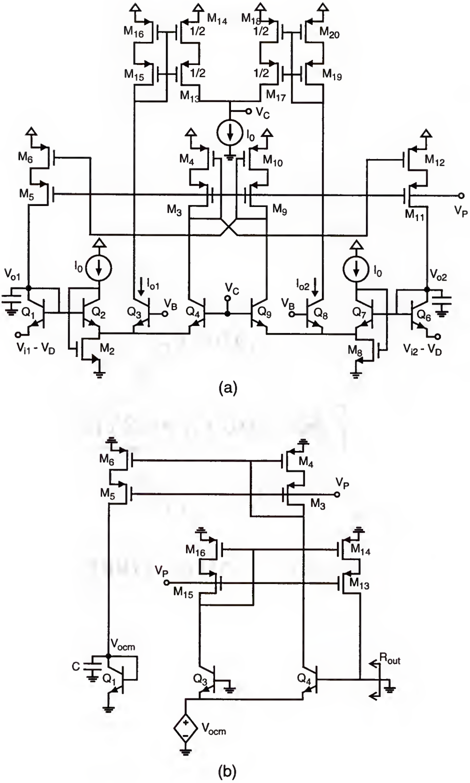
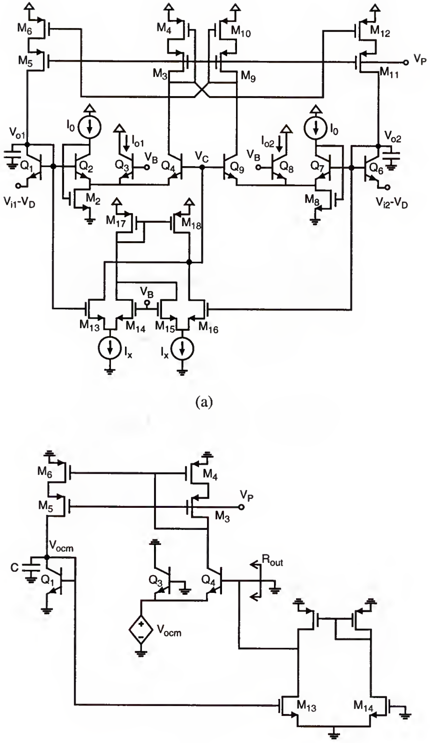


Figure 4.10 (a) Differential integrator with the arithmetic-mean CMFB. (b) Small-signal common-mode equivalent circuit.



(a)

(b)

Figure 4.11 (a) Differential log-domain integrator with the geometric-mean CMFB. (b) Small-signal common-mode equivalent circuit.

$$I_{o2} = \frac{\sqrt{i_{out}^2 + 4I_0^2} - i_{out}}{2}, \tag{4.35}$$

where i_{out} is the bandpass or lowpass output current computed from the filter's linear transfer functions. The closed-form solutions (4.34) and (4.35) are the same as (4.6) and (4.7) derived in a geometric-mean current splitter. We can also write

$$i_{out} = I_0 exp[(V_B - V_{o1})/V_t] - I_0 exp[(V_B - V_{o2})/V_t] = 2I_0 sinh(v_{out}/V_t), \tag{4.36}$$

where $v_{out} = V_B - V_{o1} = -(V_B - V_{o2})$, which leads to

$$I_{o1} = I_0 exp[asinh(+v_{out}/V_t)] \tag{4.37}$$

$$I_{o2} = I_0 exp[asinh(-v_{out}/V_t)]. \tag{4.38}$$

Thus the filters based on this structure are closely related to the "sinh" filter [Fre96b].

4.4.4 Harmonic-Mean CMFB

One more CMFB circuit, which can provide lower peak E cell currents than the previous circuits, is shown in Figure 4.12. The output voltages V_{o1} and V_{o2} are used to derive currents I_0^2/I_{o1} and I_0^2/I_{o2}, which are the collector currents of Q_{10} and Q_{11}, respectively. These are summed, and forced (for infinite CM loop gain) to equal $2I_0$, forcing the harmonic mean $1/[(1/I_{o1}) + (1/I_{o2})]$ to equal $I_0/2$. Therefore,

$$\frac{1}{\frac{1}{I_{o1}} + \frac{1}{I_{o2}}} \cong \frac{I_0}{2}. \tag{4.39}$$

If, during a signal peak, $I_{o1} >> I_0$, the constant harmonic mean implies that the peak amplitude of I_{o2} approaches $I_0/2$ rather than zero (as in the constant-geometric-mean case). The increased minimum amplitude of I_{o1} or I_{o2} reduces the peak internal current in the second-order filter, since the internal current is $(I_0 I_{i1})/I_{o1}$ or $(I_0 I_{i2})/I_{o2}$, as shown in (4.30) and (4.31). Solving (4.3) and (4.39) in terms of I_{o1} and I_{o2} yields the closed-form solutions

$$I_{o1} = \frac{1}{2}\left(\sqrt{i_{out}^2 + I_0^2} + I_0 + i_{out}\right) \tag{4.40}$$

$$I_{o2} = \frac{1}{2}\left(\sqrt{i_{out}^2 + I_0^2} + I_0 - i_{out}\right). \tag{4.41}$$

The closed-form solutions for differential output currents allow the prediction of the peak internal currents using (4.30) and (4.31). The first terms in the parentheses of (4.30) and (4.31) are the internal currents. The internal output currents of E_{L1}^+ and E_{L2}^+ in Figure 4.8 are

$$I_{EL1}^+ = I_0 \frac{I_{oB1}}{I_{oL1}} \tag{4.42}$$

and

$$I_{EL2}^+ = I_0 \frac{I_{oB2}}{I_{oL2}}, \tag{4.43}$$

where I_{oL1} and I_{oL2} denote I_{o1} and I_{o2} at the lowpass output port, and I_{oB1} and I_{oB2} denote those at the bandpass output port. (4.42) and (4.43) predict the peak value of the internal currents by substituting the values of I_{o1} and I_{o2} from the closed-form solutions into (4.42) and (4.43). This prediction can be used to determine E cell topologies and transistor geometries for a set of filter specifications without repeated nonlinear circuits simulations.

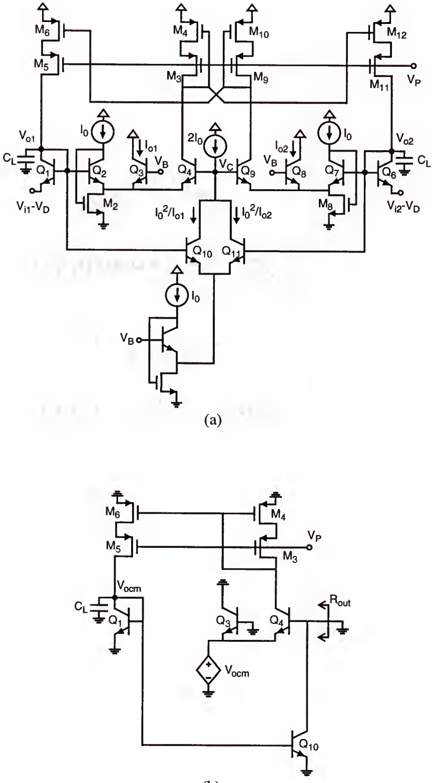


Figure 4.12 (a) Differential log-domain integrator with the harmonic-mean CMFB. (b) Small-signal equivalent circuit.

4.4.5 CMFB Small-Signal Analysis

The low frequency CM mode gain T_{01} in the circuit without the CMFB (see Figures 4.5 and 4.7) is approximately unity. The new CMFB circuits can be analyzed using the small-signal CM half-circuits in Figures 4.10 (b), 4.11 (b), and 4.12 (b). The gains of the added CMFB loops can be expressed as $T_{02} = G_{mc}R_{out}$, where R_{out} is the resistance to ground at the V_C node in the CM half-circuit, and G_{mc} is the transconductance of a transistor in the loop. In the arithmetic-mean circuit (see Figure 4.10), G_{mc} is the common-base transconductance of Q_3 (or Q_8) times the unity current gain through M_{15} - M_{13} (or M_{19} - M_{17}) and equals g_{m0}, where $g_{m0} = I_0/V_t$. In the geometric-mean CMFB circuit (see Figure 4.11), the transconductance G_{mc} is that of the actively loaded source-coupled pair, and equals the transconductance of M_{13} or M_{14} (or M_{15} or M_{16}). Note that the gain of the CMFB circuit could be increased by substituting NPNs for the n-channel MOS (NMOS) FET differential pairs or by varying their tail current I_x in Figure 4.11. In the harmonic-mean circuit (see Figure 4.12), G_{mc} is the common-emitter transconductance of Q_{10} (or Q_{11}) and equals $g_{m0} = I_0/V_t$. In all three circuits, load resistance R_{out} includes current-source output resistances and also includes $r_{\pi 4}$, so T_{02} is no higher than the current gain β of Q_4.

Since these loop gains are fairly high, it is important to consider stability. Two common-mode loops are superposed. One of the loops already exists when no CMFB circuit is added, and another loop is formed by adding a CMFB circuit. A zero is generated in the integrator due to the superposition of two common-mode loops. Thus, the common-mode loop gain of the integrator is

$$T(s) = \frac{(T_{01} + T_{02})(1 + s/\omega_z)}{(1 + s/\omega_{P_1})(1 + s/\omega_0)}, \qquad (4.44)$$

where the dominant pole frequency ω_{P_1} is given by

$$\omega_{P_1} = \frac{1}{R_{out}C_P}, \qquad (4.45)$$

and the second pole at the filter cutoff frequency by

$$\omega_0 = \frac{g_{m0}}{C_L}. \qquad (4.46)$$

Here, C_L is the integrating capacitance, C_P is the total parasitic capacitance at the V_C node in the CM half-circuit. The zero

$$\omega_Z \cong \frac{G_{mc}}{C_P} \cong GBW = \omega_{P_1}(T_{01} + T_{02}) \cong \omega_{P_1}T_{02} \qquad (4.47)$$

where T_{02} is assumed to be much greater than T_{01}. Above ω_0, there is additional phase shift due to other parasitic effects, especially delays through the PMOS current mirrors. The unity-loop-gain frequency typically lies somewhere between ω_z and ω_0, as shown in Figure 4.13 (a) and (b). Assuming the parasitic phase effects are small at ω_0, the CMFB circuits even without compensation are unlikely to be unstable. However, to ensure adequate phase margin, ω_z cannot be much higher than ω_0. (Figure 4.13 (c) shows the unstable condition.) Equivalently, C_{total} (total capacitance at V_C node) should not be much less than $(G_{mc}/g_{m0})C_L$ or else common-mode stability and transient response may be degraded. Therefore, a compensation capacitor C_C may need to be added at the high-impedance node V_C to increase the total capacitance C_{total}.

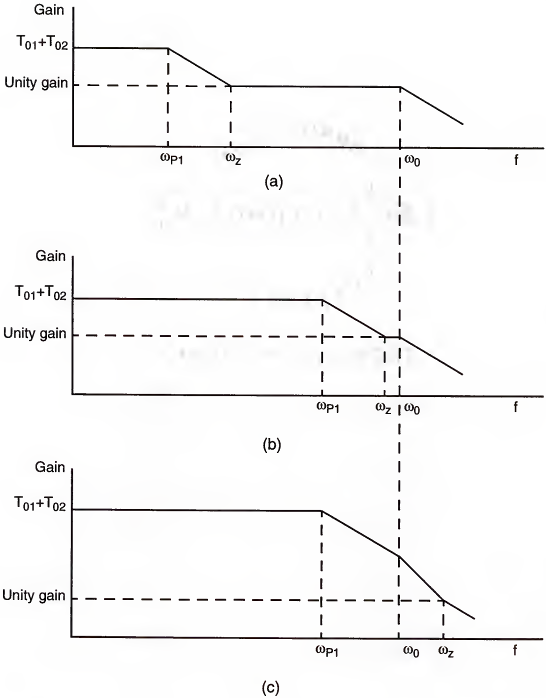


Figure 4.13 Frequency response of the CM loop of a typical integrator with CMFB when (a) $\omega_z < \omega_0$. (b) $\omega_z >$ (or =) ω_0. (c) $\omega_z >> \omega_0$.

Figure 4.14 shows results of the phase margin of an integrator with the harmonic-mean CMFB versus the ratio C_C/C_L. As expected, for fixed C_L, the phase margin increases as C_C increases. For large C_L, the circuit tends to be stable even for small C_C. However, for smaller C_L, parasitic phase effects become more important and C_C must be increased to get good phase margin.

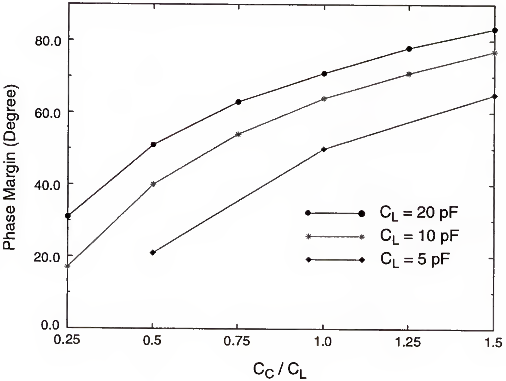


Figure 4.14 Simulated CMFB phase margin for various values of compensation and load capacitances.

4.5 Simulation and Experimental Results

Three differential second-order lowpass/bandpass log-domain filters were designed, based on the differential integrator in Figure 4.7. In one of the designs, no CMFB was added. The other two filters had geometric-mean CMFB circuits or harmonic-mean CMFB circuits at both bandpass and lowpass ports.

4.5.1 Simulation Results

The filters were simulated using HSPICE with the following model parameters: supply voltage V_{DD} = 3 V, reference current I_0 = 15 μA, C = 5 pF, center frequency f_0 = 19 MHz, Q = 1. All BJTs were modeled in HSPICE using β = 95, VAF = 47.7 V, TF = 4.7 ps, CJE = 11.9 fF, CJC = 23.0 fF, and CJS = 7.1 fF. MOSIS 1.5 μm BISIM3 models were used for the MOSFETs. The NMOS FETs had W = 96 μm, L = 2.4 μm, AD = AS = 384 $(\mu m)^2$, and the PMOS FETs, which compose the current mirrors in E^- cells, had W = 58.4 μm, L = 2.4 μm, AD = AS = 232 $(\mu m)^2$. 10 pF shunt capacitors were added at the V_C nodes in the harmonic-mean CMFB loops, providing about 50° CM phase margin.

Figure 4.15 shows the simulation results of the frequency responses at the lowpass and the bandpass output ports of the differential second-order log-domain filter without CMFB circuits. The cutoff/center frequency was 19 MHz, as expected, and the dc gains of the lowpass output and the bandpass output were unity and -44 dB, respectively.

Figure 4.16 shows the waveforms of the internal currents $I_{E1}{}^+$ at the lowpass part of the filters when no CMFB circuit was added, when the geometric-mean CMFB circuits were added, and when the harmonic-mean CMFB circuits were added, respectively. The input signal frequency was 500 Hz, and the modulation index was 20. From the filter structure in Figure 4.8, the internal output current of $E_1{}^+$ at the lowpass part

$$I_{EL1}{}^+ = I_0 \frac{I_{oB2}}{I_{oL1}} \tag{4.48}$$

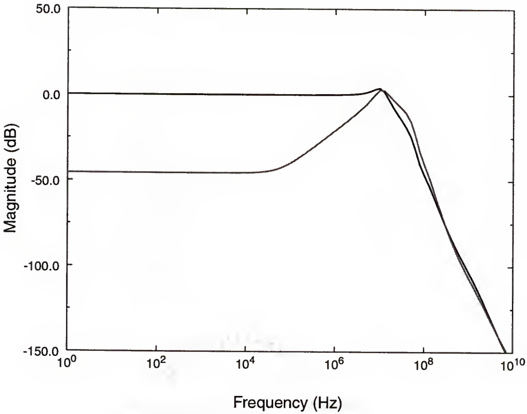


Figure 4.15 Frequency responses of the differential second-order log-domain lowpass/bandpass filter from HSPICE simulations.

(4.48) shows that the largest minimum value of I_{oL1} produces the smallest value of $I_{EL1}{}^{+}$. Therefore, as expected, the peak value of the internal current of the filter with the harmonic-mean CMFB circuits was least since the minimum value of I_{oL1} of the filter was largest among those three filters. The waveform of $I_{EL1}{}^{+}$, when no CMFB was added, was clipped, since the transistor geometries of the current mirrors in E^- cells could not accommodate the large current. HSPICE can show an instantaneous operating point at any time during a signal period. The operating point of the filter without added CMFB at 500 μs verified that the PMOS transistors in E^- cells had entered in the triode region.

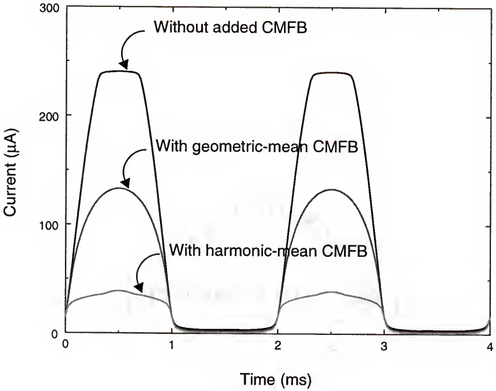


Figure 4.16 Simulated internal current waveforms at the lowpass port in differential second-order filters with/without CMFB circuits when $V_{DD} = 3$ V.

Figure 4.17 shows THD at the lowpass output port versus modulation index for three filters. When *m* was between one and 16, the THD levels of the three filters were not much different since the peak values of all $I_{EL1}{}^{+}$ currents were not large enough to overload the PMOS FETs in the E⁻ cells. When *m* was equal to 20, the THD of the filters without the added CMFB, with the geometric-mean CMFB, and with the harmonic-mean CMFB were 1.73%, 0.54%, and 0.39%, respectively. As *m* increases, THD of the filter without the CMFB increased steeply due to the severe clipping of $I_{EL1}{}^{+}$.

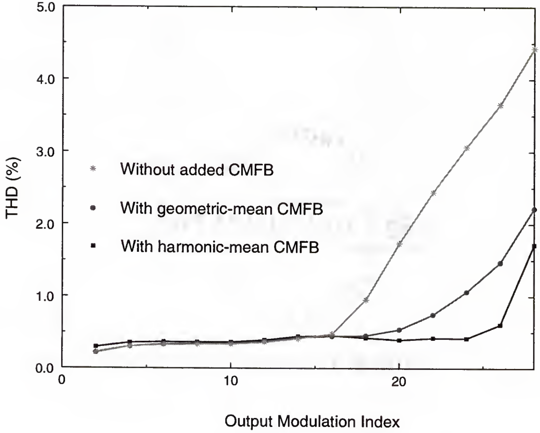


Figure 4.17 Comparison of THD (through simulations) of the lowpass output vs. modulation index of the filters with the harmonic-mean CMFB, with the geometric-mean CMFB, and without the added CMFB.

Figure 4.18 shows THD simulations for the three filters when the supply voltage V_{DD} was changed from 3 V to 2.4 V, with all other filter specifications unchanged. The obvious difference between Figure 4.17 and Figure 4.18 is the THD of the filter with the harmonic-mean CMFB. The plot shows a "bump" around $m = 8$. This bump was related to overload in the level-shifters composed of Q_2 and M_7 (or Q_7 and M_8) in Figure 4.12 (a). There was not much voltage headroom for Q_2, since the collector voltage of Q_2 was equal to the V_{GS} of M_2 and V_B equals 1 V. This distortion mechanism can be eliminated by redesigning the E cells, as shown in

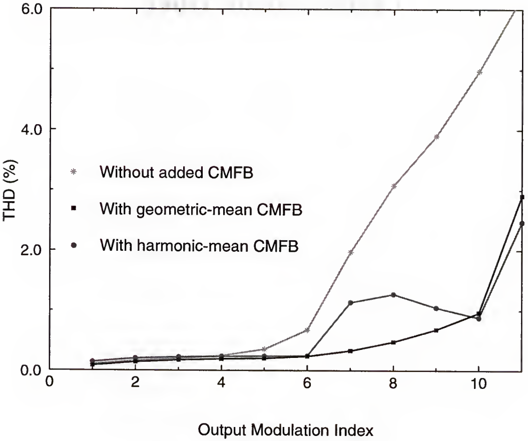


Figure 4.18 Comparison of THD (through simulations) of the lowpass output vs. modulation index of the filters with the harmonic-mean CMFB, with the geometric-mean CMFB, and without the added CMFB, when V_{DD} = 2.4 V.

Figure 2.9. The THD of the filter without the added CMFB increased from less than 0.5% for m = 5 to over 3% for m = 8. When the harmonic-mean or geometric-mean CMFB was added at both the lowpass and bandpass ports, THD stays below 1.5% for m up to 10. For $m \geq 10$, THD in the filter with geometric-mean CMFB tends to be larger than in the filter with harmonic-mean CMFB, due to the larger internal current $I_{EL1}{}^{+}$. Figure 4.19 shows the current waveforms of each $I_{EL1}{}^{+}$ in three filters when m = 8 and V_{DD} = 2.4 V. The hump that appears on the current waveform of $I_{EL1}{}^{+}$ of the filter with the harmonic-mean CMFB was caused by overload in the level shifters,

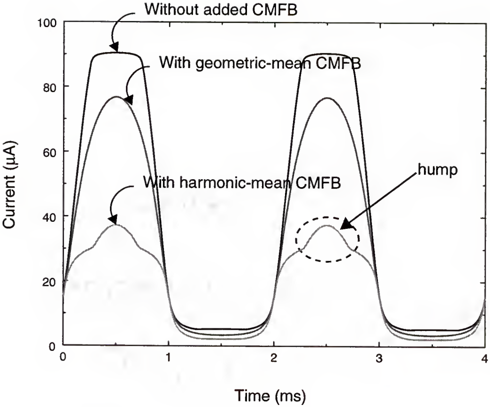


Figure 4.19 Simulated internal current waveforms at the lowpass port in differential second-order filters with/without CMFB circuits when $V_{DD} = 2.4$ V.

increasing the distortion. The hump on the current waveform appears for *m* larger than six, and dominates the THD for *m* from six to 10, as shown in Figure 4.18.

4.5.2 Experimental Results

The filters were built in the MOSIS AMI ABN 1.5 µm CMOS process, which provides rudimentary NPN BJTs without buried collector layer, as shown in Figure 4.20. The emitter and base were designed using a finger-type layout to decrease parasitic resistance [Ro99]. The test chip contained the three differential second-order lowpass/bandpass filters simulated in the previous section. Figure 4.21 shows the test chip layout of the filters. Electrostatic discharge (ESD) protection

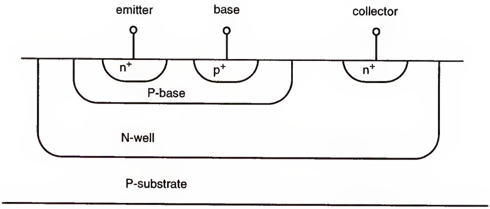


Figure 4.20 NPN BJT provided by the MOSIS AMI ABN 1.5 μm process.

diodes were included for all pads. The chip size including the pads was 2200 μm x 2200 μm. The upper part of the chip is the filter with the harmonic-mean CMFB circuits, the middle part is the filter with the geometric-mean CMFB circuits, and the lower part is the filter without the added CMFB circuits. Two 10 pF compensation capacitors, shown in the upper-right side of Figure 4.21, were added to ensure stability of the filter with harmonic-mean CMFB.

The dc tests were performed using a parameter analyzer (HP 4155) to verify the trends predicted through simulations, including significantly reduced peak currents and enhanced linearity provided by the CMFB circuits. Differential dc input currents were injected directly from the parameter analyzer to the differential input ports of the filters. The power supply voltage was set to 2.4 V, and bias voltage V_B was set to 1.0 V. The output differential currents (I_{out1} and I_{out2}) were measured using the HP 4155 at the lowpass output ports, as functions of the dc differential input current. The output signal (I_{out}) was derived by subtracting the two differential output currents. Figure 4.22 shows the output signal versus modulation index for the

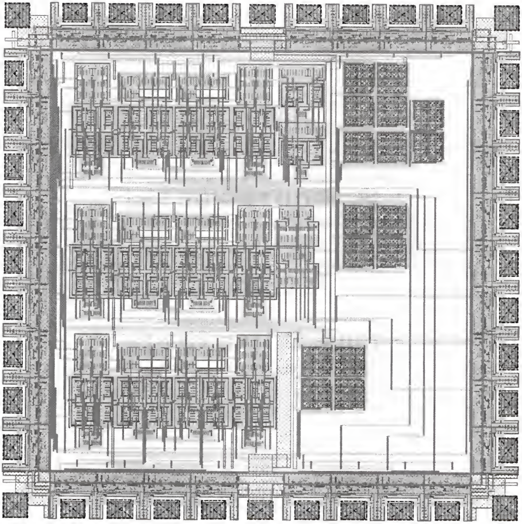


Figure 4.21 Differential second-order lowpass/bandpass filter layout. Three filters were placed in one chip.

filters without added CMFB, with the geometric-mean CMFB circuits, and the harmonic-mean CMFB circuits, when the tunable bias current I_0 was set to 11 μA, 15 μA, and 20 μA, respectively. In Figure 4.22, constant slope would indicate linear output current. As the slope decreases with increasing modulation index, the output current is nonlinear.

To highlight the effects of the CMFB circuits on the internal currents, Figure 4.22 was converted to Figure 4.23, which shows the gain of the filters versus modulation index. If the gain is constant, the output currents are linear, and when the gain starts decreasing, nonlinear output currents were produced by the clipping of the internal currents. The lowpass gain was designed as unity, thus the constant gain shown in Figure 4.23 should be unity. However, the constant gains from the measurement results were slightly higher than unity, most likely due to process variations.

A printed circuit board (PCB) for a 40-pin chip was designed and used for ac measurements. Figure 4.24 shows a detailed measurement setup. An AC voltage signal is injected to a transformer by a function generator (HP3311A). The transformer produces two voltage signals 180° out of phase for the differential inputs of a filter. A dc blocking capacitor (C = 0.1 μF) is connected directly to the output of the transformer, and a resistor (R = 10 kΩ) is placed between the capacitor and an input port of a filter converts an ac voltage signal to a current signal. At the output stage, the output currents I_{o1} and I_{o2} are converted into voltages by resistors (R = 10 kΩ) and connected to a digital oscilloscope (Agilent 54622D) for

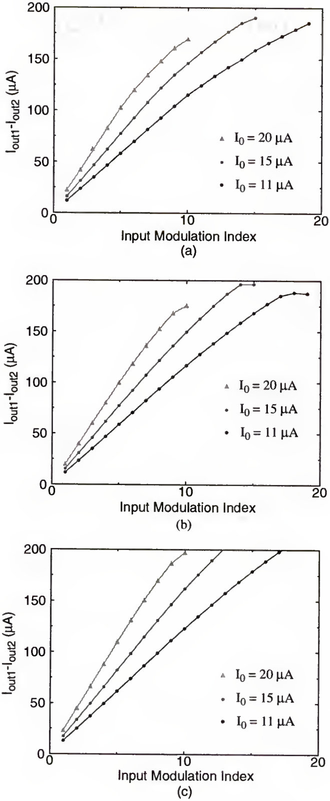


Figure 4.22 Measured output currents vs. input modulation index. The filter (a) without the added CMFB, (b) with the geometric-mean CMFB, (c) with the harmonic-mean CMFB.

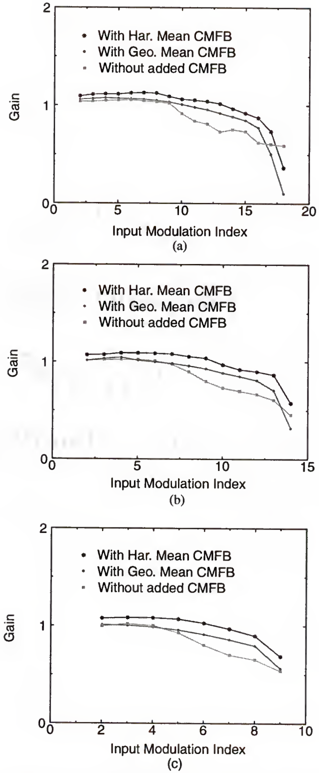


Figure 4.23 Measured lowpass output gain dI_{outLP} / dI_{in} vs. modulation index when (a) $I_0 = 11$ μA, (b) $I_0 = 15$ μA, and (c) $I_0 = 20$ μA.

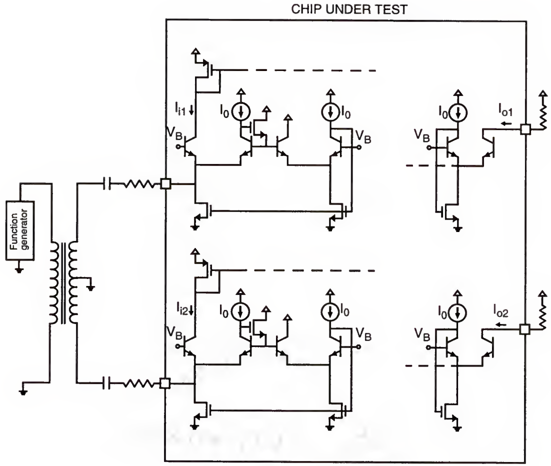


Figure 4.24 AC measurement setup of the test chip.

measurements. Bias voltages were supplied from a dc power supplier. Figure 4.25 shows the actual measurement setup on a printed circuit board.

Figure 4.26 shows typical measured lowpass and bandpass frequency responses. All the filters had similar frequency responses. Bias current I_0 was set to 1 μA, which ideally would yield a cutoff/center frequency of 1.2 MHz. The measured cutoff/center frequency was slightly less than the ideal value, most likely due to inadequate modeling of parasitic effects. (The BJTs used were never fully characterized.) The cutoff/center frequency variation can be tuned by varying the

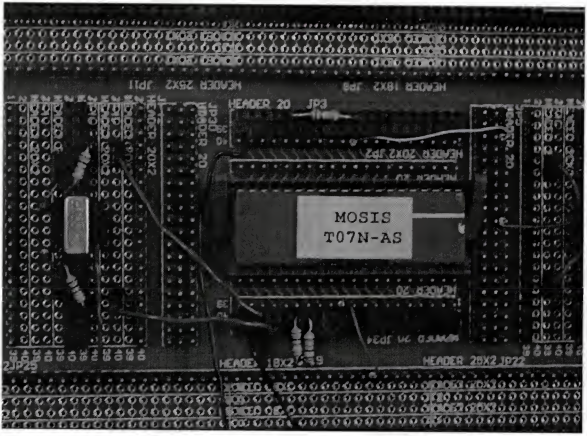


Figure 4.25 Actual measurement setup on a printed circuit board.

bias current of the filter. The deviation in filter Q from its designed value (1.0) and the modest low-frequency attenuation for the bandpass response are attributable to mismatch, which could probably have been lowered through more careful layout. The figure shows signal feedthrough around 10 MHz, probably because of inadequate input/output isolation in the test setup.

4.6 Conclusions

Although differential log-domain filters can operate Class AB, resulting in infinite dynamic range ideally, in practical applications, the maximum signal swing is limited by E cell topology and transistor geometries. CMFB circuits can be added to differential second-order log-domain filters without affecting external

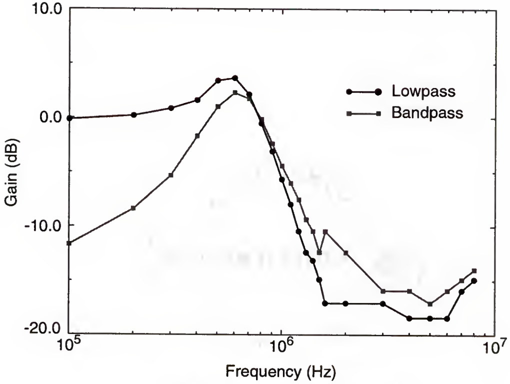


Figure 4.26 Measured frequency responses of differential second-order lowpass/bandpass filter with tunning current $I_0 = 1\ \mu A$.

linearity. Two useful CMFB circuits have been proposed: the geometric-mean CMFB circuit and the harmonic-mean CMFB circuit. The CMFB circuits reduce the peak internal currents in log-domain filters, reducing nonlinearity. These CMFB circuits allow increased signal swing of the log-domain filters and increasing the dynamic range. Simulation and experimental results were given.

CHAPTER 5
DIFFERENTIAL LOG-DOMAIN FILTERS WITH MIXED COMMON-MODE FEEDBACK

5.1 Introduction

The differential second-order log-domain filter composed of two differential log-domain integrators has lowpass and bandpass output ports, as shown in Figure 4.8. CMFB circuits can be added at both output ports, forcing the differential output currents to follow simple forms.

In the previous chapter, the same CMFB circuits were added at both bandpass and lowpass ports of the second-order filters. This chapter explores the possibility of applying CMFB to only one of the two stages within a differential second-order log-domain bandpass/lowpass filter. Closed-form expressions are found for the peak currents in such filters, for the case of low input frequency. Circuits that have the lowest peak currents for low frequency inputs are usually the best choices overall for linearity, because low frequencies correspond to the highest peak currents. Also, low frequencies are worst-case for harmonic distortion, since there is no removal of higher harmonics by the filter.

With two integrator stages and three possible CMFB arrangements (geometric-mean CMFB, harmonic-mean CMFB, and no added CMFB) at each integrator output, there are nine possible combinations. In the nine possible implementations, the peak E^+ cell currents at the bandpass and the lowpass ports will be estimated to find which combination of the CMFB circuits produce the minimum peak value.

5.2 Internal E+ Cell Currents

The differential second-order log-domain filter, based on interconnecting E cells, has bandpass and lowpass output ports, as shown in Figure 4.8. The linear output currents i_{outBP} and i_{outLP} are

$$i_{outBP} = I_{oB1} - I_{oB2} \tag{5.1}$$

and

$$i_{outLP} = I_{oL1} - I_{oL2}. \tag{5.2}$$

At frequencies low enough that capacitive currents can be neglected, the nodal equation at V_{oB1} is given by

$$\frac{I_0 I_{i1}}{I_{oB1}} + \frac{I_0 I_{oL1}}{I_{oB1}} = \frac{I_0}{Q} + I_{oB2} \cdot f_B(I_{oB1}, I_{oB2}), \tag{5.3}$$

where $f_B(I_{oB1}, I_{oB2}) = exp[(V_{CB} - V_B)/V_t]$. Multiplying both sides of (5.3) by I_{oB1}/I_0 yields

$$I_{i1} + I_{oL1} = \frac{I_{oB2}^2}{I_0} f_B(I_{oB1}, I_{oB2}) + \frac{I_{oB1}}{Q}, \tag{5.4}$$

and the nodal equation at V_{oB2} is leads to

$$I_{i2} + I_{oL2} = \frac{I_{oB1}^2}{I_0} f_B(I_{oB1}, I_{oB2}) + \frac{I_{oB2}}{Q}. \tag{5.5}$$

The nodal equations at V_{oL1} and V_{oL2} at low frequencies yield

$$I_{oB1} = I_{oB2} = \frac{I_{oL1} I_{oL2}}{I_0} \cdot f_L(I_{oL1}, I_{oL2}), \tag{5.6}$$

where $f_L(I_{oL1}, I_{oL2}) = exp[(V_{CL} - V_B)/V_t]$. Note that $f_B(I_{oB1}, I_{oB2}) = f_L(I_{oL1}, I_{oL2}) = 1$ when no CMFB circuit is added at either port, since V_{CB} and V_{CL} are connected to V_B. Therefore, if no CMFB circuit is added at the lowpass port, from (5.6),

$$I_{oB1} = I_{oB2} = \frac{I_{oL1} I_{oL2}}{I_0}. \tag{5.7}$$

In Figure 4.8, the voltage signals V_{oL1} and V_{oB1} are applied at the positive and the negative input ports of E_{B1}^+, respectively. The output current of E_{B1}^+ does not appear externally, but the current exists internally. Using the sinking E^+ cell's function in (2.3) and the translinear principle, the current can be expressed as

$$I_{EB1}^+ = I_0 exp\left(\frac{V_{oB1} - V_{oL1}}{V_t}\right) = I_0 \frac{I_{oL1}}{I_{oB1}}, \tag{5.8}$$

where

$$I_{oB1} = I_0 exp\left(\frac{V_B - V_{oB1}}{V_t}\right) \tag{5.9}$$

and

$$I_{oL1} = I_0 exp\left(\frac{V_B - V_{oL1}}{V_t}\right). \tag{5.10}$$

The output currents of the other E^+ cells are

$$I_{EB2}^+ = I_0 exp\left(\frac{V_{oB2} - V_{oL2}}{V_t}\right) = I_0 \frac{I_{oL2}}{I_{oB2}}, \tag{5.11}$$

$$I_{EL1}^+ = I_0 exp\left(\frac{V_{oL1} - V_{oB2}}{V_t}\right) = I_0 \frac{I_{oB2}}{I_{oL1}}, \tag{5.12}$$

and

$$I_{EL2}^{\ +} = I_0 exp\left(\frac{V_{oL2} - V_{oB1}}{V_t}\right) = I_0 \frac{I_{oB1}}{I_{oL2}}, \tag{5.13}$$

where $I_{EB2}^{\ +}$, $I_{EL1}^{\ +}$, and $I_{EL2}^{\ +}$ are the internal output currents of $E_{B2}^{\ +}$, $E_{L1}^{\ +}$, and $E_{L2}^{\ +}$, respectively, and

$$I_{oB2} = I_0 exp\left(\frac{V_B - V_{oB2}}{V_t}\right) \tag{5.14}$$

and

$$I_{oL2} = I_0 exp\left(\frac{V_B - V_{oL2}}{V_t}\right). \tag{5.15}$$

5.3 Mixed CMFB Circuits

Three CMFB circuits, the arithmetic-mean CMFB circuit, the geometric-mean CMFB circuit, and the harmonic-mean CMFB circuit, have been proposed for differential second-order log-domain lowpass/bandpass filters. In this chapter, only the geometric-mean CMFB circuit and the harmonic-mean CMFB circuit will be considered for the combinations of the CMFB circuits since the arithmetic-mean CMFB circuit does not allow Class AB operation.

The geometric-mean CMFB circuit shown in Figure 4.11 provides a pair of closed-form solutions for the differential output currents, as shown in (4.34) and (4.35). Substituting the maximum value of $i_{out} = mI_0 sin(\omega t)$ into (4.34) and (4.35) yields

$$I_{o1} = \frac{\sqrt{i_{out}^{\ 2} + 4I_0^{\ 2}} + i_{out}}{2} = \frac{\sqrt{m^2 I_0^{\ 2} + 4I_0^{\ 2}} + mI_0}{2} = I_0\left(\sqrt{\frac{m^2}{4} + 1} + \frac{m}{2}\right) \tag{5.16}$$

and

$$I_{o2} = \frac{\sqrt{i_{out}^2 + 4I_0^2} - i_{out}}{2} = \frac{\sqrt{m^2 I_0^2 + 4I_0^2} - mI_0}{2} = I_0\left(\sqrt{\frac{m^2}{4} + 1} - \frac{m}{2}\right). \qquad (5.17)$$

Using the Taylor's binomial series

$$(a + x)^n \approx a^n + na^{n-1}x, \qquad (5.18)$$

for $a^2 \gg x^2$, therefore,

$$\sqrt{\frac{m^2}{4} + 1} \approx \left(\frac{m^2}{4}\right)^{\frac{1}{2}} + \frac{1}{2}\left(\frac{m^2}{4}\right)^{\frac{1}{2} - 1} = \frac{m}{2} + \frac{1}{m}. \qquad (5.19)$$

Substituting (5.19) into (5.16) and (5.17) yields the approximate maximum values of

$$I_{o1} \approx I_0\left(\frac{m}{2} + \frac{1}{m} + \frac{m}{2}\right) = I_0\left(m + \frac{1}{m}\right) \qquad (5.20)$$

and

$$I_{o2} \approx I_0\left(\frac{m}{2} + \frac{1}{m} - \frac{m}{2}\right) = \frac{I_0}{m}. \qquad (5.21)$$

For $m \geq 2$, the error in the approximation of the peak I_{o1} is less than 4%.

The closed-form solutions for the harmonic-mean CMFB circuit (4.40) and (4.41) are

$$I_{o1} = \frac{1}{2}\left(\sqrt{i_{out}^2 + I_0^2} + I_0 + i_{out}\right) = \frac{I_0}{2}\left(\sqrt{m^2 + 1} + 1 + m\right) \qquad (5.22)$$

and

$$I_{o2} = \frac{1}{2}\left(\sqrt{i_{out}^2 + I_0^2} + I_0 - i_{out}\right) = \frac{I_0}{2}\left(\sqrt{m^2 + 1} + 1 - m\right). \qquad (5.23)$$

Using the Taylor's binomial series in (5.18), for m greater than about 2, yields

$$\sqrt{m^2 + 1} \approx m + \frac{1}{2m}. \qquad (5.24)$$

Substituting (5.24) into (5.22) and (5.23) yields approximate maximum values of

$$I_{o1} \approx I_0\left(m + \frac{1}{2} + \frac{1}{4m}\right) \tag{5.25}$$

and

$$I_{o2} \approx I_0\left(\frac{1}{2} + \frac{1}{4m}\right). \tag{5.26}$$

For $m \geq 2$, the error in the approximation of the peak I_{o1} is less than 0.3%.

There are nine possible ways to combine the CMFB circuits for the bandpass and the lowpass output ports of the filter shown in Figure 4.8 with two CMFB circuits and without the added CMFB circuit. The nine combinations are: (A) the geometric-mean CMFB circuits are added at both lowpass and bandpass ports (GG); (B) the geometric-mean CMFB circuit is added at the bandpass port, and the harmonic-mean CMFB circuit is added at the lowpass port (GH); (C) the harmonic-mean CMFB circuit is added at the bandpass port, and the geometric-mean CMFB circuit is added at the lowpass port (HG); (D) the harmonic-mean CMFB circuits are added at both lowpass and bandpass ports (HH); (E) the geometric-mean CMFB circuit is added at the bandpass port, and no CMFB circuit is added at the lowpass port (GN); (F) no CMFB circuit is added at the bandpass port, and the geometric-mean CMFB circuit is added at the lowpass port (NG); (G) the harmonic-mean CMFB circuit is added at the bandpass port, and no CMFB circuit is added at the lowpass port (HN); (H) no CMFB circuit is added at the bandpass port, and the harmonic-mean CMFB circuit is added at the lowpass port (NH); and (I) no CMFB circuit is added at either the bandpass or the lowpass port (NN). Figures 5.1 and 5.2

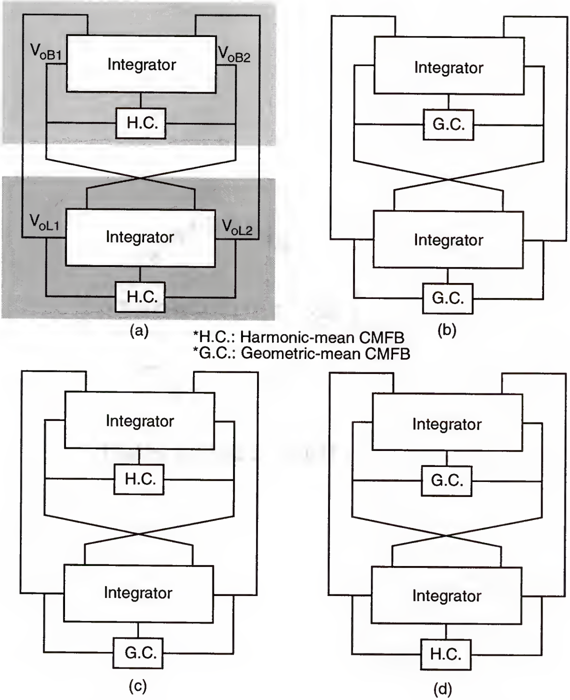


Figure 5.1 Differential second-order bandpass/lowpass filters with (a) H.C. at the bandpass and the lowpass ports, (b) G.C. at the bandpass and the lowpass ports, (c) H.C. at the bandpass port and G.C. at the lowpass port, and (d) G.C. at the bandpass port and H.C. at the lowpass port. The current splitter is not shown.

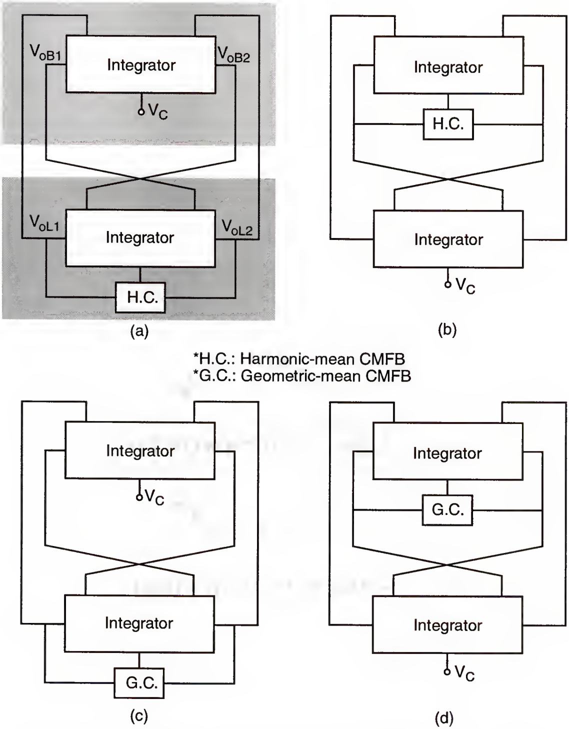


Figure 5.2 Differential second-order bandpass/lowpass filters with (a) H.C. at the lowpass port, (b) H.C. at the bandpass port, (c) G.C. at the lowpass port, and (d) G.C. at the bandpass port. The current splitter is not shown. V_C is the bias voltage that is converted to I_0 when there is no input signal.

show eight of the nine possible implementations of the second-order differential filters, excluding the NN case.

The nine combinations can be divided into four groups, based on the approaches needed to solve for the differential output currents:

(A) If infinite loop-gain CMFB circuits are added at both the bandpass and the lowpass ports, then $I_{oB1}, I_{oB2}, I_{oL1}$, and I_{oL2} can be predicted by (5.20), (5.21), (5.25), and (5.26). The GG, GH, HG, and HH cases belong to this group.

(B) In the GN and HN cases, $f_L(I_{oL1}, I_{oL2}) = 1$, and the feedback forces $I_{oB1} = I_{oB2} = I_0$, since $i_{outBP} = 0$. Substituting these values into (5.6) yields $I_{oL1}I_{oL2} = I_0^2$. Therefore, the differential output currents I_{oL1} and I_{oL2} can be predicted by (5.20) and (5.21), the equations for the currents in the geometric-mean CMFB circuit.

(C) In the NG case, $I_{oL1}I_{oL2} = I_0^2$ because of the added geometric-mean CMFB circuit at the lowpass port, and thus I_{oL1} and I_{oL2} are given by (5.20) and (5.21). Substituting $f_B(I_{oB1}, I_{oB2}) = 1$ into the nodal equation (5.5) gives

$$\frac{I_{oB}^2}{I_0} + \frac{I_{oB}}{Q} - I_{i2} - I_{oL2} = 0, \qquad (5.27)$$

where $I_{oB1} = I_{oB2} = I_{oB}$. Substituting the approximate peak amplitude $\frac{I_0}{Q}\left(m + \frac{1}{m}\right)$ and $\frac{I_0}{m}$ into I_{i2} and I_{oL2} in (5.27), respectively, gives a quadratic formula in terms of I_{oB}. Note that the closed-form solutions for the geometric-mean CMFB circuit can be applied to the differential input currents I_{i1} and I_{i2} since $I_{i1}I_{i2} = I_0^2/Q$, when $I_{Ref} = I_0/Q$ in the current splitter. Solving the quadratic formula yields

$$I_{oB,\,MAX} = -\frac{I_0}{2Q} + \frac{I_0}{2}\sqrt{\frac{1}{Q^2} + 4\left(\frac{m}{Q} + \frac{1}{Qm} + \frac{1}{m}\right)}. \tag{5.28}$$

In the NH case, $(I_{oL1}I_{oL2})/(I_{oL1} + I_{oL2}) = I_0/2$ by the added harmonic-mean CMFB circuit at the lowpass port, and thus I_{oL1} and I_{oL2} can be predicted. The nodal equation (5.5) is expressed in the form of (5.27) since $f_B(I_{oB1}, I_{oB2}) = 1$, as in the NG case. Substituting the approximate peak amplitude $\frac{I_0}{Q}\left(m + \frac{1}{m}\right)$ and $I_0\left(\frac{1}{2} + \frac{1}{4m}\right)$ into I_{i2} and I_{oL2}, respectively, gives a quadratic formula in terms of I_{oB}. Solving the formula yields

$$I_{oB} = -\frac{I_0}{2Q} + \frac{I_0}{2}\sqrt{\frac{1}{Q^2} + 4\left(\frac{m}{Q} + \frac{1}{Qm} + \frac{1}{4m} + \frac{1}{2}\right)}. \tag{5.29}$$

(D) In the NN case, $f_B(I_{oB1}, I_{oB2}) = 1$ and $f_L(I_{oL1}, I_{oL2}) = 1$. Substituting $f_L(I_{oL1}, I_{oL2}) = 1$ in (5.6) gives

$$I_{oB} = \frac{I_{oL1}I_{oL2}}{I_0} = \frac{(I_{oL2} + mI_0)I_{oL2}}{I_0} = \frac{I_{oL2}^{\;2}}{I_0} + mI_{oL2}, \tag{5.30}$$

where $I_{oL1} = I_{oL2} + mI_0$ at dc. Substituting the quadratic formula from the right side of (5.30) into I_{oB} in (5.4) and (5.5) leads to a fourth-order polynomial formula in terms of I_{oL1} or I_{oL2}, which cannot be solved in convenient closed form.

5.4 Simulation Results

In many simulations of differential second-order bandpass/lowpass log-domain filters, overload of the current mirrors in the E^- cells was the dominant cause of distortion. The overload of the current mirrors was caused by the nonlinear internal output currents of E^+ cells. This suggests that circuits that minimize the largest E-cell currents will provide the lowest distortion.

5.4.1 Idealized Simulations

To verify the relations derived in the previous section, the computed peak currents were compared to idealized simulations performed using MATLAB and HSPICE. For HH, GG, HG, and GH cases, MATLAB simulations were performed with the closed-form solutions and the E^+ cell current equations shown in (5.8) and (5.11) through (5.13). The filter cutoff/center frequency was set to 18.4 MHz and $Q = 1$, respectively. The applied input signal frequency was 500 Hz, and the peak E^+ cell currents were estimated for various modulation indices.

For the GN, HN, NG, HG, and NN cases, idealized HSPICE simulations were performed on the filters to provide estimates of the peak magnitudes of the E^+-cell currents. These simulations used extremely large W/L and simple Level-1 model parameters for MOSFETs, and infinite β and V_A for BJTs. The filter specifications were identical with those used for the MATLAB simulations. The tuning current I_0 was set to 15 μA, and integrating capacitors were set to 5 pF to give the cutoff/center frequency of 18.4 MHz.

Figure 5.3 shows the normalized peak E^+ cell currents versus modulation index for the GG, GH, HG and HH cases, where the normalized values were calculated by dividing the actual current values by I_0. Figure 5.3 (a) and (d) show the lowest peak magnitudes of ${I_{EL1}}^+$ and ${I_{EB2}}^+$ for the modulation index m up to 30, and Figure 5.3 (b) and (c) show the highest peak magnitudes of ${I_{EL2}}^+$ and ${I_{EB1}}^+$. Figure 5.4 shows the normalized peak E^+ cell currents of the GN, NG, HN, NH, and NN cases from the idealized HSPICE simulations.

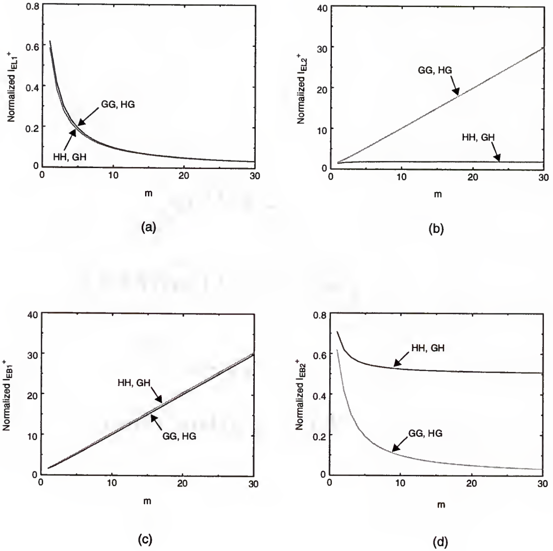
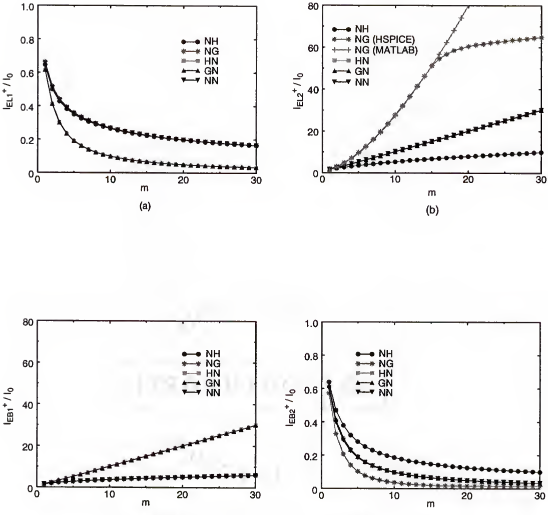


Figure 5.3 MATLAB simulation results of the normalized internal E^+ cell currents versus modulation indices. (a) $I_{EL1}{}^+$. (b) $I_{EL2}{}^+$. (c) $I_{EB1}{}^+$. (d) $I_{EB2}{}^+$.



(a)

(b)

(c)

(d)

Figure 5.4 HSPICE simulation results of the normalized internal E^+ cell currents versus modulation indices. (a) I_{EL1}^+. (b) I_{EL2}^+. (c) I_{EB1}^+. (d) I_{EB2}^+.

Figures 5.3 (b) and 5.4 (b) show that the normalized peak magnitudes of $I_{EL2}{}^{+}$ of the NH, HH, and GH cases were smaller than the other six cases for *m* up to 30. The NG case showed such large $I_{EL2}{}^{+}$ that there was clipping of PMOS FET current mirrors in the E^- cells in the HSPICE simulation, even though the simulations were idealized. Figures 5.3 (c) and 5.4 (c) show that the NH case has lower peak magnitudes of $I_{EB1}{}^{+}$ than the HH and GH cases. Therefore, the NH case gives a good compromise, providing low maximum values of both $I_{EL2}{}^{+}$ and $I_{EB1}{}^{+}$. This suggests that the NH case may offer large signal swings in practical circuits, with large dynamic range and low THD.

5.4.2 Practical Simulations

More realistic HSPICE simulations were performed to estimate THD for practical filters using the NN, HH, and NH cases. The circuits used the following model parameters: supply voltage V_{DD} = 3 V, reference current I_0 = 15 µA, C = 5 pF, center/cutoff frequency f_0 = 19 MHz, $Q = 1$. All BJTs were modeled in HSPICE using β = 95, VAF = 47.7 V, TF = 4.7 ps, CJE = 11.9 fF, CJC = 23.0 fF, and CJS = 7.1 fF. The MOSIS 1.5 µm BISIM3 models were used for the MOSFETs. The NMOS FETs had W = 96 µm, L = 2.4 µm, AD = AS = 384 $(\mu m)^2$, and the PMOS FETs, which compose the current mirrors in E^- cells, had W = 58.4 µm, L = 2.4 µm, AD = AS = 232 $(\mu m)^2$.

Figure 5.5 shows the simulated THD versus *m* for the NN, NH, and HH cases. THD of these three cases were not much different for *m* between 1 and 16, staying below 0.5%. The THD of the NN case started to increase sharply when *m* was

16, producing THD higher than 1.5% when *m* was equal to 20, whereas the THD levels for the NH case stayed below 1% for *m* up to 23 and in the HH case to about 27.

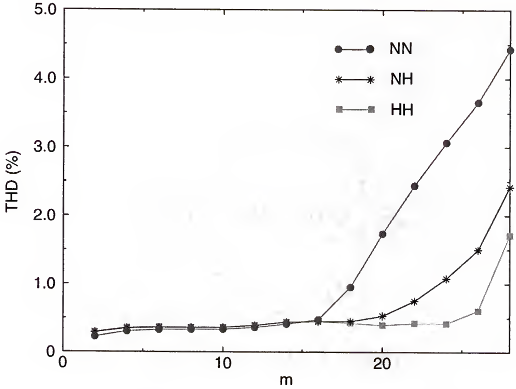


Figure 5.5 Comparison of THD vs. modulation index of the NN, NH, and HH cases.

5.5 Conclusions

With three possible CMFB arrangements at each integrator output of a differential second-order bandpass/lowpass log-domain filter, nine possible combinations were proposed. In simulations of a wide variety of transistor-level of circuits implementing these filters, the HH and NH cases consistently have better dynamic range than other combinations. However, the detailed results depend strongly on the circuit implementation, and are not perfectly correlated with the ideal analysis presented here.

CHAPTER 6
GENERALIZATION OF DESIGN METHODOLOGIES FOR LOG-DOMAIN FILTERS

6.1 Introduction

Chapters 2 and 3 presented methods for designing log-domain integrators, first-order filters, and single-ended second-order filters based on E cells. The design methodology for log-domain filters can be further generalized. A filter transfer function can be converted to a signal flow graph (SFG) [Che95] composed of nodes, branches, and the weights of the branches. When a G_m-C filter is implemented from an SFG, each branch is converted to a transconductor and the transconductances are proportional to the corresponding weights.

A log-domain filter can be implemented from a current-mode G_m-C filter by replacing transconductors with E cells. However, direct replacement is not possible, since the output conductance of an ideal transconductor is zero, whereas an E cell has a nonzero output conductance equal to the transconductance of the E cell. Therefore, the output conductance of an E cell is proportional to the corresponding weight in a log-domain filter SFG. Also, at the zero-signal operating point, an E cell's output current is proportional to its output conductance, and thus, is also proportional to the corresponding weight.

This chapter shows three ways to convert a current-mode G_m-C filter to a corresponding log-domain filter. The first way is to replace each transconductor with a zero-output-conductance log-domain transconductor equivalent. The second way is to replace each transconductor with an E cell whose bias current is proportional to the transconductance, and, if necessary, to add a feedback-connected E cell (whose one input is tied to the bias voltage V_B) to adjust the net output conductance at each integrator output node. The third approach is to scale the weights of the E cells in a log-domain filter SFG, which can allow redundant circuits to be eliminated.

An E cell has at least one pair of BJTs or weak-inversion MOSFETs. One transistor is tied to an input (and will be called an input transistor), and another is tied to the output (and will be called an output transistor). The weight of an E cell is proportional to its transconductance, which is also proportional to its output conductance and to the current in the output transistor at the zero-signal operating point. Therefore, setting the weights yields a set of output bias currents for the E cells at their zero-signal operating points. However a the input bias currents of the E cells are not necessarily determined by the weights. To determine the input bias currents, two biasing strategies can be used. One of them is the simple biasing strategy already used in the previous chapters, in which the input and output transistors in each E cell carry the same current at the zero-signal operating point. Also, it has been assumed that all of the transistors have equal area, so the V_{BE}'s are the same at the zero-signal operating point, so that the same dc voltage appears at the input and the output of an E cell. An alternate biasing strategy is to identify translinear loops and to vary the input bias currents while satisfying the current-mode translinear equations. This biasing strategy can allow simpler filter circuits without changing the transfer function.

6.2 Design of Log-Domain Filter from Current-Mode Gm-C Filter

6.2.1 Signal Flow Graph

Consider a voltage-mode transfer function given by

$$H(s) = \frac{I_o}{I_i} = \frac{b_m s^m + b_{m-1} s^{m-1} + \ldots + b_1 s + b_0}{s^n + a_{n-1} s^{n-1} + \ldots + a_1 s + a_0}, \; m \le n. \tag{6.1}$$

For $n = 3$ and $m = 2$, (6.1) becomes

$$H(s) = \frac{b_2\left(\frac{1}{s}\right) + b_1\left(\frac{1}{s}\right)^2 + b_0\left(\frac{1}{s}\right)^3}{1 + a_2\left(\frac{1}{s}\right) + a_1\left(\frac{1}{s}\right)^2 + a_0\left(\frac{1}{s}\right)^3}. \tag{6.2}$$

If s is normalized by a cutoff frequency ω_0, then

$$s' = \frac{s}{\omega_0}. \tag{6.3}$$

Substituting $s = s'\omega_0$ into (6.2) yields

$$H(s) = \frac{\frac{b_2}{\omega_0}\left(\frac{1}{s'}\right) + \frac{b_1}{\omega_0^2}\left(\frac{1}{s'}\right)^2 + \frac{b_0}{\omega_0^3}\left(\frac{1}{s'}\right)^3}{1 + \frac{a_2}{\omega_0}\left(\frac{1}{s'}\right) + \frac{a_1}{\omega_0^2}\left(\frac{1}{s'}\right)^2 + \frac{a_0}{\omega_0^3}\left(\frac{1}{s'}\right)^3} = \frac{b_2'\left(\frac{1}{s'}\right) + b_1'\left(\frac{1}{s'}\right)^2 + b_0'\left(\frac{1}{s'}\right)^3}{1 + a_2'\left(\frac{1}{s'}\right) + a_1'\left(\frac{1}{s'}\right)^2 + a_0'\left(\frac{1}{s'}\right)^3}, \tag{6.4}$$

where all b_i' and a_j', for $i = j = 0, 1, 2$, are dimensionless. Figure 6.1 shows an observer canonical form SFG [Kai80] for (6.2). The primes are omitted for simplicity in Figure 6.1.

6.2.2 Implementation of a Current-Mode Gm-C Filter from an SFG

An SFG as shown in Figure 6.1 can be used to design a voltage-mode G_m-C filter. To convert a SFG into a voltage-mode G_m-C filter, each $1/s$ in the SFG is replaced by a grounded capacitor value of g_{m0}/ω_0, each branch with the weight of 1

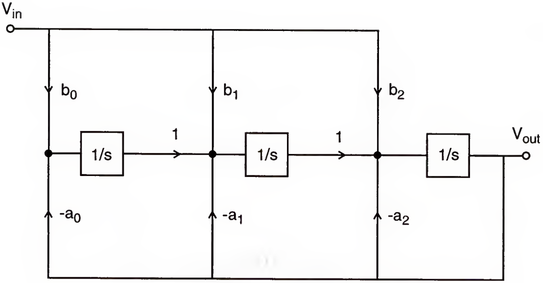


Figure 6.1 Observer canonical form SFG for $n = 3$ and $m = 2$.

is replaced by a transconductor of value g_{m0}, and each branch with the weight of a_i and b_j is replaced by a transconductor of value $a_i g_{m0}$ and $b_j g_{m0}$, where $i = j = 0, 1, 2$. For example, Figure 6.2 shows a third-order voltage-mode G_m-C filter designed based on Figure 6.1. Three G_m-C integrators are implemented by the transconductors with the grounded capacitors.

Note that a voltage-mode G_m-C filter can be converted to a current-mode G_m-C filter by adding a feedback-connected transconductor for converting an input current to a voltage, and a output transconductor for converting an output voltage to a current [Geo99], as shown in Figure 6.3. Figure 6.4 shows a third-order current-mode G_m-C filter converted from the voltage-mode G_m-C filter shown in Figure 6.2.

6.2.3 Conversion of Gm-C filters to Log-Domain Filters

The transconductor whose transconductance is proportional to b_0 can be converted to a log-domain equivalent composed of a sourcing E^+ cell and a sinking

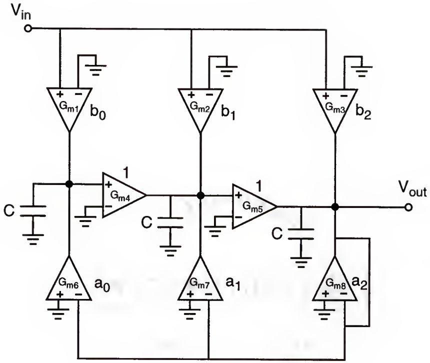
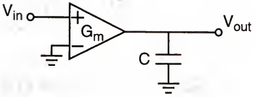
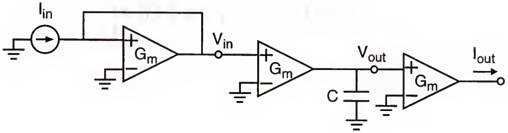


Figure 6.2 Third-order voltage-mode G_m-C filter, assuming the values of capacitors are equal.

E^- cell whose bias currents are equal to each other, and proportional to b_0, as shown in Figure 6.5 The V_+ and V_- inputs in the transconductor can be realized by the V_+ input of the E^+ cell and the V_- input of the E^- cell. At the zero-signal operating point, the dc output current of the E^+ cell is sunk by the E^- cell. In small-signal analysis, zero net output conductance at V_{out} in Figure 6.5 (b) realizes the infinite output impedance of an ideal transconductor. Therefore, each of the transconductors G_{m1}, G_{m2}, G_{m3}, G_{m4}, G_{m5}, G_{m6}, G_{m7}, and G_{m10} in Figure 6.4 can be converted to a log-domain equivalent composed of a pair of E cells. To provide damping, the negative-feedback-connected G_{m8} is replaced by a dc current source whose value is



(a)



(b)

Figure 6.3 G_m-C integrators. (a) Voltage-mode integrator and (b) Current-mode integrator.

proportional to a_2. Directly converting the transconductors to their log-domain equivalents produces a cumbersome and complex circuit.

A relatively simple transistor-level log-domain transconductor equivalent is shown in Figure 6.6 [Pyt01, Ser02]. This circuit is based on the E$^+$ cell and E$^-$ cell shown in Figures 2.3 and 2.4. The output current

$$I_{out} = I_1 - I_2 = I_0\left[exp\left(\frac{V_+ - V_{out}}{V_t}\right) - exp\left(\frac{V_- - V_{out}}{V_t}\right)\right]. \qquad (6.5)$$

At the zero-signal operating point (V_+ and V_- are connected to a bias voltage V_B, and no signal is applied to V_+ and V_- ports), $I_1 = I_2$, so $I_{out} = 0$. Transistors Q_3, M_1, and Q_2 form a positive feedback loop, and Q_3, M_1, Q_1, M_2, and M_3 form a negative

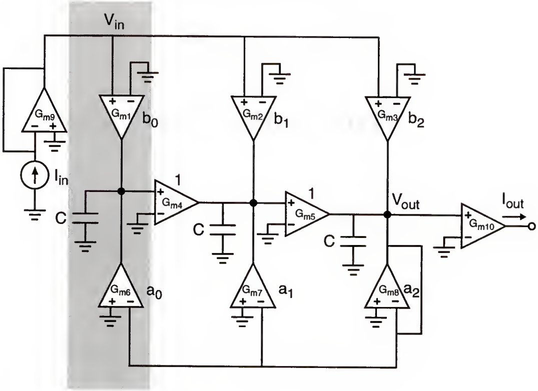
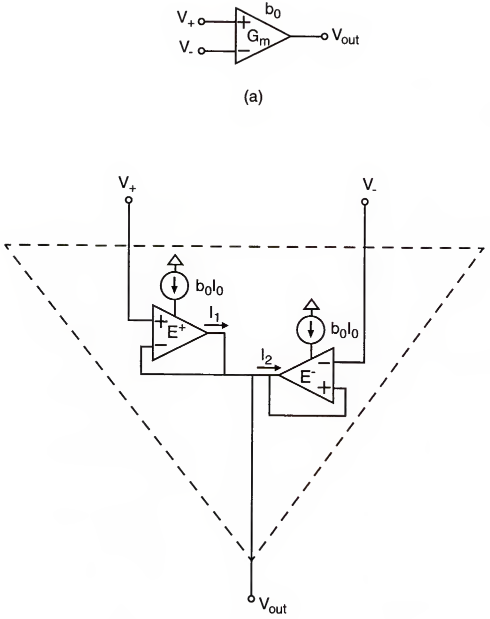


Figure 6.4 Third-order current-mode G_m-C filter, assuming the values of capacitors are equal.

feedback loop, producing zero net output conductance at the output node. This circuit is attractive, since the E^+ cell and E^- cell share a level-shifter composed of Q_3 and M_1, reducing the filter complexity.

Another way to convert a G_m-C filter to a log-domain filter is to replace each transconductor with an E cell whose bias current is proportional to the corresponding transconductance. For example, each transconductor in the highlighted part in Figure 6.4 is replaced by an E cell. Assume that sourcing E^+ cells and sinking E^- cells are being used. Then the noninverting transconductor G_{m1} is replaced by a sourcing E^+ cell, and the inverting transconductor G_{m6} is replaced by a sinking E^- cell, where the bias currents of the E cells are proportional to the



(a)

(b)

Figure 6.5 (a) Transconductor whose transconductance is proportional to b_0. (b) Log-domain equivalent of the transconductor shown in (a).

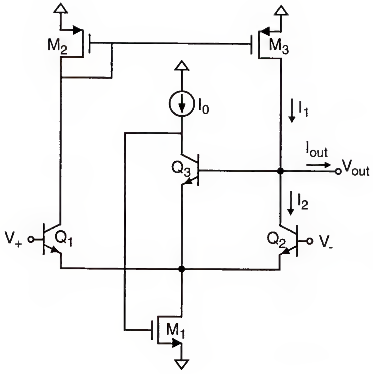
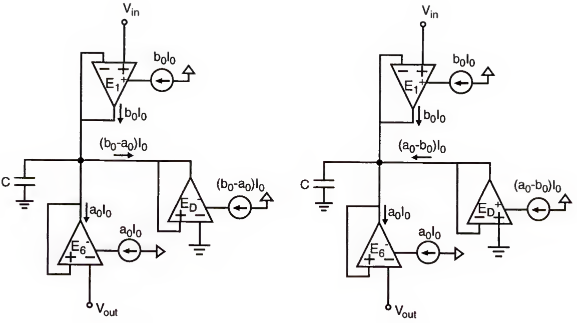


Figure 6.6 A transistor-level log-domain equivalent of a transconductor.

corresponding transconductances b_0 and a_0, respectively. At the dc operating point, the E$^+$ cell sources output current equals to its bias current b_0I_0 and the E$^-$ cell sinks output current a_0I_0. The difference of b_0I_0 and a_0I_0 would produce damping. To eliminate the damping, a "dummy" E cell (a feedback-connected cell with one input tied to the V_B bias source) should be added to sink the difference current. If $b_0 > a_0$, then the positive difference current $(b_0\text{-}a_0)I_0$ should be sunk by a positive-feedback-connected dummy E$^-$ cell whose bias current is $(b_0\text{-}a_0)I_0$, as shown in Figure 6.7 (a). If $a_0 > b_0$, then a negative-feedback-connected dummy E$^+$ cell added at the integrating node should source the positive difference current $(a_0\text{-}b_0)I_0$, as shown in Figure 6.7 (b). If $a_0 = b_0$, then no dummy E cell is needed. In small-signal analysis,



(a) (b)

Figure 6.7 Log-domain equivalent of the highlighted part of the G_m-C filter shown in Figure 6.4 when (a) $b_0 > a_0$ and (b) $a_0 > b_0$.

when $b_0 > a_0$, the positive net output conductance of E_1^+ and E_6^- is cancelled by the negative output conductance of E_D^-. For $a_0 > b_0$, the negative net output conductance of E_1^+ and E_6^- is cancelled by the positive output conductance of E_D^+, resulting in zero net output conductance. The transconductors G_{m3} and G_{m8} are replaced by E^+ cells, sourcing the output currents $b_2 I_0$ and I_0, respectively. To provide the damping, the current $(b_2+1-a_2)I_0$ should be sunk by an added dummy E^- cell, and the balance $a_2 I_0$, by a fixed current sink.

The above conversion methods use more E cells than the number of transconductors, as shown in Figures 6.5 and 6.7. To reduce the number of necessary E cells, and design simpler log-domain filters, a scaling method can be used, which scales the weight of E cells or capacitors in an SFG without varying the overall transfer function. Figure 6.8 (a) shows a part of a log-domain filter SFG including four E cells and the corresponding weights *a*, *b*, *c*, and *d*. The bias currents and input ports (V_+ and V_-) of the E cells in Figure 6.8 were omitted for simplicity. If the weights of all the E cells driven by V_C are multiplied by a constant scale factor K, then the weights of all the E cells driving V_C should be divided by the same scale factor K simultaneously. The amplitude of signals at V_C are scaled by K, but transfer functions to all other nodes are unchanged. Therefore, the weights *a* and *d* should be divided by *K*, as shown in Figure 6.8 (b). An alternate approach is to scale the capacitor C. Figure 6.8 (c) shows that the weights *b* and *c* and capacitor C are all multiplied by K, whereas the weights of E_1 and E_4 are unchanged.

An example of scaling the weights of a log-domain filter SFG will be shown with Figure 6.9 which was converted from Figure 6.4 by replacing the transconductors with E cells. The weights of E_1, E_2, and E_3 are multiplied by a_0/b_0 to make the sum of the weights of E_1 and E_6 zero. Simultaneously, the weight of E_{out} is divided by a_0/b_0, as shown in Figure 6.10. At the zero-signal operating point, the output current of E_1 is sunk by E_6. At the damping node V_{out}, the sum of the weights of E_3 and E_5 must equal a_2. Thus the weight of E_5 is multiplied by $(a_2-b_2a_0/b_0)$, and the weights of E_2, E_4, and E_7 are divided by $(a_2-b_2a_0/b_0)$, as shown in Figure 6.11. At the zero-signal operating point, the sum of the output currents of E_2 and E_4 is sunk by E_7. Finally, the sum of the weights of E_2, E_4, and E_7 at node V_2 must equal zero. Thus, the weight of E_4 is multiplied by $(a_1-b_1a_0/b_0)$ and the weights of E_1 and E_7 are divided by the same factor, as shown in Figure 6.12. Figure 6.13 shows the SFG

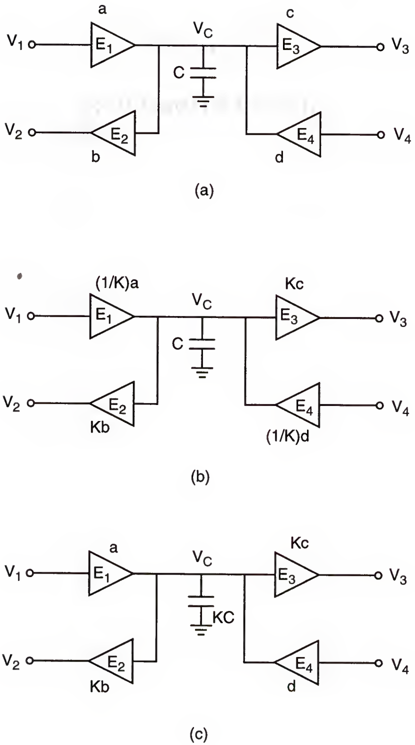


Figure 6.8 Scaling SFG. (a) An SFG. (b) Scaling by varying the weights. (c) Scaling by varying the capacitor.

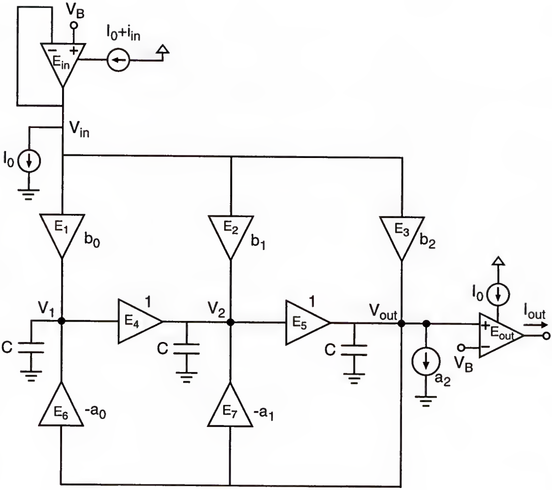


Figure 6.9 The SFG of a third-order log-domain filter converted from a third-order current-mode G_m-C filter shown in Figure 6.4.

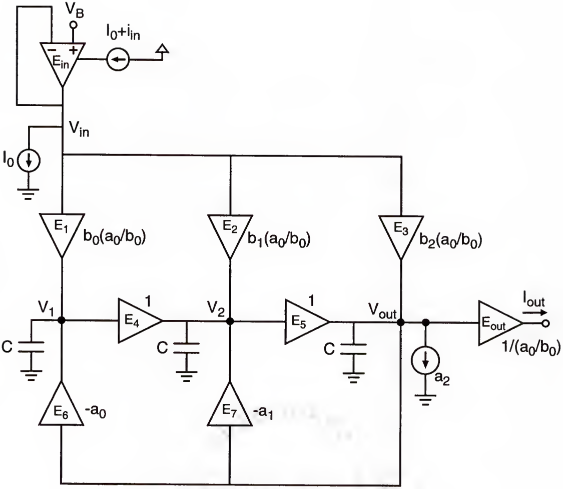


Figure 6.10 The SFG scaled by multiplying the weights of E_1, E_2, and E_3 by a_0/b_0 and dividing the weight of E_6 by the same factor from the SFG shown in Figure 6.9.

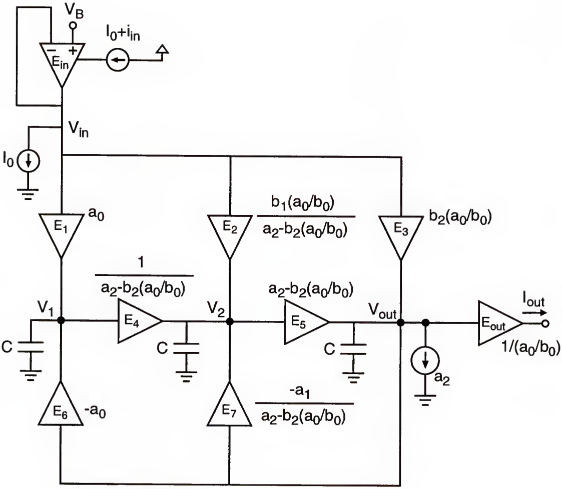


Figure 6.11 The SFG scaled by multiplying the weights of E_5 by a_2-$b_2(a_0/b_0)$ to make the sum of the weights of E_3 and E_5 equal a_2. The weights of the corresponding input E cells, E_2, E_4, and E_8, are divided by the same factor.

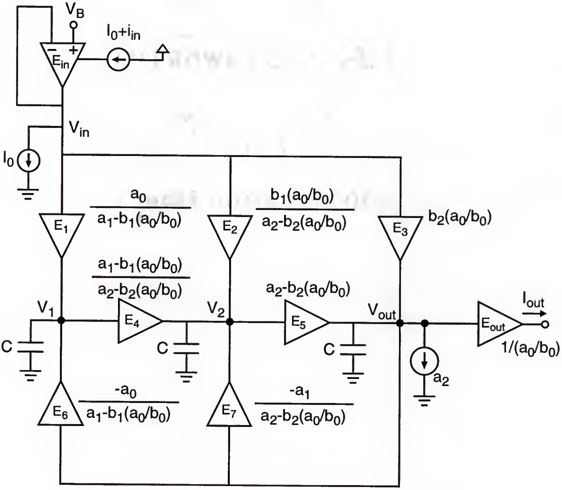


Figure 6.12 The SFG scaled by multiplying weight of E_4 by a_1-$b_1(a_0/b_0)$ to make the sum of the weights of E_2, E_4, and E_8 equal zero. The weights of the corresponding input E cells, E_1 and E_7, are divided by the same factor.

redrawn from Figure 6.12 by replacing the E cells whose weights are positive with sourcing E^+ cells and the E cells whose weights are negative with sinking E^- cells. This weight scaling method eliminates dummy E cells, and thus reduces the number of E cells, resulting in a simpler circuit.

6.3 DC Biasing for Log-Domain Filters

The log-domain filter is a kind of translinear circuits that may contain several translinear loops. In log-domain filter circuits considered at the transistor level, an even number of the base-emitter junctions are interconnected to form translinear loops. Therefore, the currents in the transistors follow current-mode translinear loop equations.

6.3.1 Simple Biasing for E cells

In most of the above, a simple biasing strategy has been assumed, in which the input and output transistors in each E cell carry the same current at the zero-signal operating point. This means the input bias current of each E cell is equal to the output bias current of the E cell at the zero-signal operating point, and is proportional to the weight of the E cell. The voltages across the output transistors in each E cell are equal to the voltages across their associated input transistors, so all of the capacitor voltages are equal to the same bias voltage, V_B. This simple biasing strategy avoids the need for translinear loop analysis, and makes the circuit easy to design and to debug. However, simpler circuits may be possible in some cases, if an alternate biasing strategy is followed.

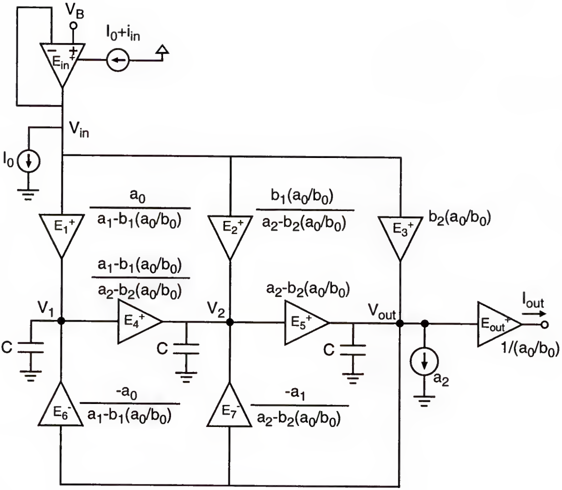


Figure 6.13 The SFG of a third-order log-domain filter.

6.3.2 Alternate Biasing for E cells

Figure 6.14 shows a third-order log-domain filter implemented from Figure 6.13 by replacing the E^+ and E^- cells with the transistor-level circuits shown in Figures 2.1 (c) and 2.8 (c). The output bias currents of all E cells, I_{x1}, I_{x2}, I_{x3}, I_{x4}, I_{x5}, I_{x6}, I_{x7}, I_{x8}, and I_{x9}, are proportional to the weights of the corresponding E cells in the SFG shown in Figure 6.13. For example, the output bias current of Q_4, I_{x2}, is equal to $[(CV_t\omega_0)a_0]/[a_1-b_1(a_0/b_0)]$. The translinear loop formed by the base-emitter junctions of Q_1, Q_2, Q_7, Q_8, Q_{13}, and Q_{14} in Figure 6.14 produces a current-mode translinear loop equation

$$I_{01}I_{04}I_{07} = I_{x1}I_{x4}I_{x7}, \tag{6.6}$$

where I_{01}, I_{04}, and I_{07} represent the input bias currents of E cells. In (6.6), the product of the input bias currents equals the product of the output bias currents of Q_2, Q_8, and Q_{14}, where Q_2, Q_8, and Q_{14} are the output transistors of $E_{in}{}^+$, $E_3{}^+$, and $E_6{}^+$, respectively. In the simple biasing strategy presented in 6.3.1, I_{01} equals I_{x1}, I_{04} equals I_{x4}, and I_{07} equals I_{x7}. However, other possibilities exist. If I_{01} is decreased by a factor, the designer can increase I_{04}, I_{07}, or the product of I_{04} and I_{07} by the same factor. Therefore, the circuit designer may have the design freedom to choose the values of the input bias currents. This design freedom can allow simpler circuits, for example, when level-shifters in different E cells can be merged. (Circuit examples simplified by exploiting the design freedom will be shown later.) Also, varying the input bias currents may simplify tuning of the filter coefficients.

In a log-domain filter, many translinear loops can be identified. Among them, to produce the minimum number of translinear loop equations, the minimum

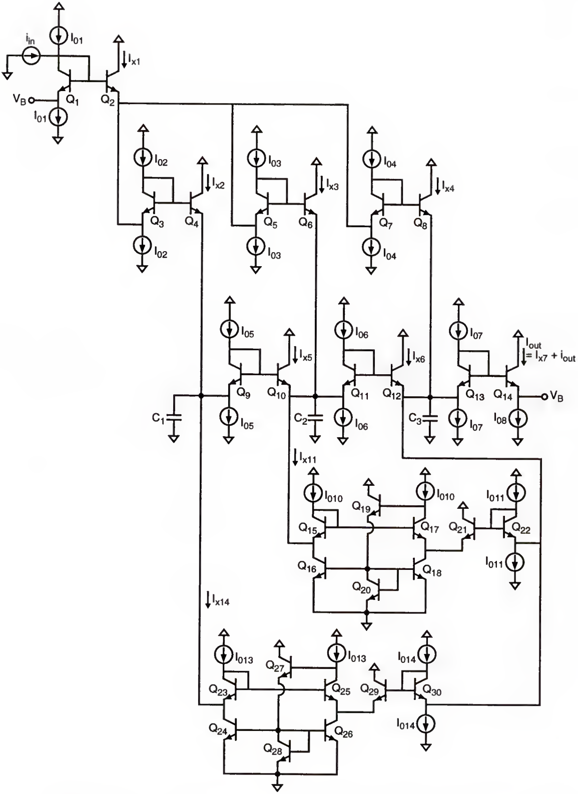


Figure 6.14 Transistor-level third-order log-domain filter based on the SFG shown in Figure 6.13.

number of independent translinear loops should be identified. To identify the independent translinear loops in a log-domain filter, a translinear loop graph can be used, which derives a relation between the topology of a translinear network and the degree of the network equations [Wie93]. An independent translinear loop does not encompass other translinear loops in the translinear loop graph. In practical conversion from a translinear circuit to a translinear loop graph, the base-emitter connections of the transistors are represented by branches in the graph [See88a], [Wie93]. The nodes in the translinear loop graph represent the connections between transistors.

The transistor-level log-domain filter shown in Figure 6.14 can be converted to a translinear graph, as shown in Figure 6.15. There are five independent translinear loops which are composed of $Q_5Q_3Q_4Q_9Q_{10}Q_6$, $Q_{14}Q_{13}Q_8Q_7Q_2Q_1$, $Q_7Q_8Q_{30}Q_{29}Q_{25}Q_{23}Q_4Q_3$, $Q_{23}Q_{25}Q_{29}Q_{30}Q_{22}Q_{21}Q_{17}Q_{15}Q_{10}Q_9$, and $Q_{15}Q_{17}Q_{21}Q_{22}Q_{12}Q_{11}$. The corresponding translinear loop equations to each translinear loop are

$$I_{03}I_{x2}I_{x5} = I_{02}I_{05}I_{x3}, \tag{6.7}$$

$$I_{07}I_{04}I_{01} = I_{x7}I_{x4}I_{x1}, \tag{6.8}$$

$$I_{04}I_{014}I_{x2} = I_{x4}I_{x14}I_{02}, \tag{6.9}$$

$$I_{x14}I_{011}I_{x5} = I_{014}I_{x11}I_{05}, \tag{6.10}$$

and

$$I_{x11}I_{x6} = I_{011}I_{06}, \tag{6.11}$$

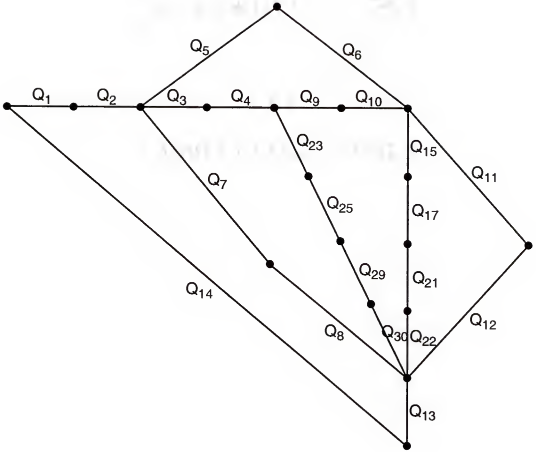


Figure 6.15 The translinear loop graph of Figure 6.14. The directions of all branches are not shown for simplicity.

respectively. Therefore, a set of input bias currents should satisfy these translinear loop equations. (Four Kirchhoff's current law equations must also be satisfied. These constraints were used in setting the E-cell output currents.)

The number of independent translinear loops can be estimated by the following equation [See88a]

$$l = b - n + 1, \tag{6.12}$$

where l is the number of independent translinear loops, b is the number of base-emitter junctions, and n is the number of nodes in a signal flow graph. In the translinear loop graph shown in Figure 6.15, b = 22 and n = 18, thus, l = 22 - 18 + 1 = 5, five independent translinear loops exist.

In the third-order log-domain filter shown in Figure 6.14, nine unknown input bias currents can be determined by five independent translinear loop equations. Thus, 9 - 5 = 4 degrees of design freedom can be given, and the design freedom can be used for simplifying four different parts of the circuit. For example, first, if I_{02} equals I_{03}, then the level-shifter Q_5 can be merged with Q_3. Second, if I_{02} equals I_{04}, the level-shifter Q_7 can be also merged with Q_3. Third, if I_{01} equals I_{02}, the level-shifter Q_1 can be merged with Q_3. Fourth, in the E^- cells, if I_{011} equals I_{014}, then the level-shifter Q_{22} can be merged with Q_{30}. Figure 6.16 shows a modified filter from Figure 6.14 by using four degrees of design freedom. Transistor Q_4 shares the level-shifter Q_1 with Q_6 and Q_8, and Q_{21} shares the level-shifter Q_{22} with Q_{29}, producing a simpler circuit.

Solving for the required values of the input bias currents requires simultaneous solution of several translinear equations. In general, the corresponding capacitor voltages will be unequal. This makes debugging such circuits much more difficult than circuits designed using the simple method described in 6.3.1.

To show another example, consider a third-order filter transfer function varied from (6.4) by forcing b_1' to equal zero, thus

$$H(s) = \frac{b_2'\left(\frac{1}{s'}\right) + b_0'\left(\frac{1}{s'}\right)^3}{1 + a_2'\left(\frac{1}{s'}\right) + a_1'\left(\frac{1}{s'}\right)^2 + a_0'\left(\frac{1}{s'}\right)^3}. \tag{6.13}$$

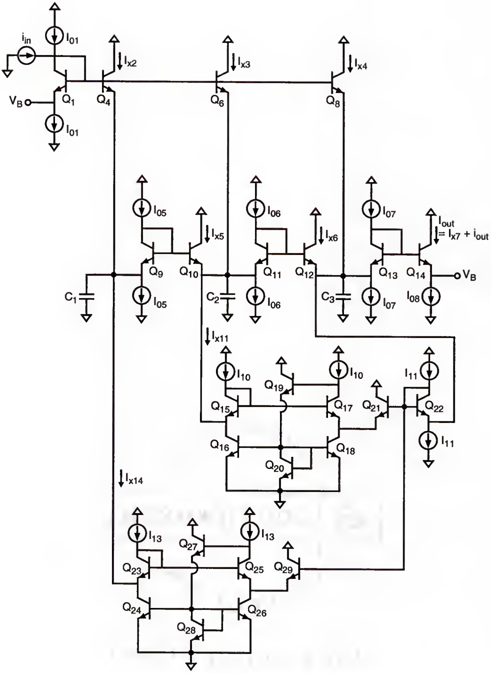


Figure 6.16 A variation of the third-order log-domain filter shown in Figure 6.14.

The zeros of the transfer function shown in (6.13) are $\pm j\sqrt{(b_0')/(b_2')}$, and are located on the imaginary ($j\omega$) axis of the s-plane. The SFG of this transfer function and a corresponding transistor-level circuit are shown in Figures 6.17 and 6.18. This circuit was derived from the circuit in Figure 6.14 by eliminating E_2^+ (Q_5 and Q_6). Thus, one degree of design freedom was used for setting b_1 to zero, leaving three more degrees of design freedom can be used for further simplification.

The weight a_2-$b_2(a_0/b_0)$ was assumed to be positive in Figure 6.17. However, this constraint is not necessary, since an E cell with a negative weight can be implemented by an E^- cell. If a_2-$b_2(a_0/b_0)$ is negative, the weights of E_4^+ and E_5^+ shown in Figure 6.17 become negative, while the weight of E_8^- becomes positive. Therefore, E_4^+ and E_5^+ should be converted to E^- cells, E_4^- and E_5^-, and E_8^- should be converted to an E^+ cell, E_8^+, as shown in Figure 6.19. Figure 6.20 shows a corresponding transistor-level circuit.

6.4 Conclusions

A design methodology for log-domain filters was generalized to allow implementation of more general transfer functions. Three ways of converting a current-mode G_m-C filter to a log-domain filter were explored. Two of them need redundant circuits to eliminate the nonzero output conductances of E cells, resulting in cumbersome circuits. Another approach involves scaling the weights of E cells in an SFG, which can eliminate redundant circuits, resulting in simpler circuits. Two dc biasing strategies were compared. In general, choosing bias currents requires simultaneous solution of several translinear loop equations. A simpler approach was

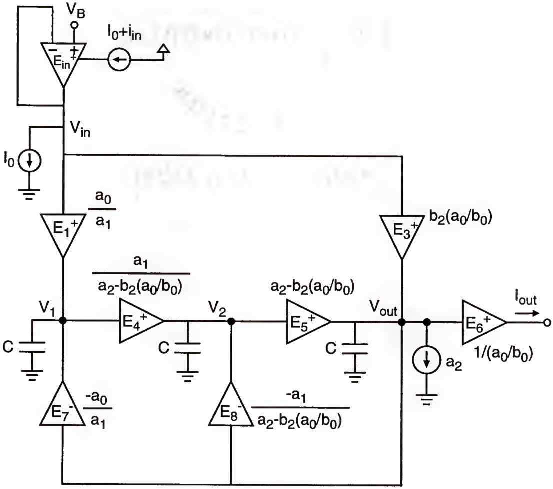


Figure 6.17 A modified SFG for $b_1 = 0$ in Figure 6.13.

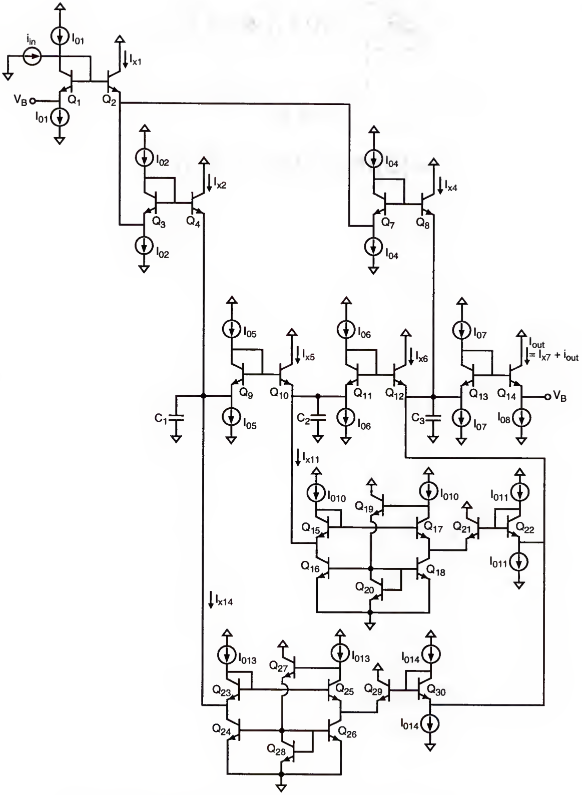


Figure 6.18 Transistor-level third-order log-domain filter based on the SFG shown in Figure 6.17.

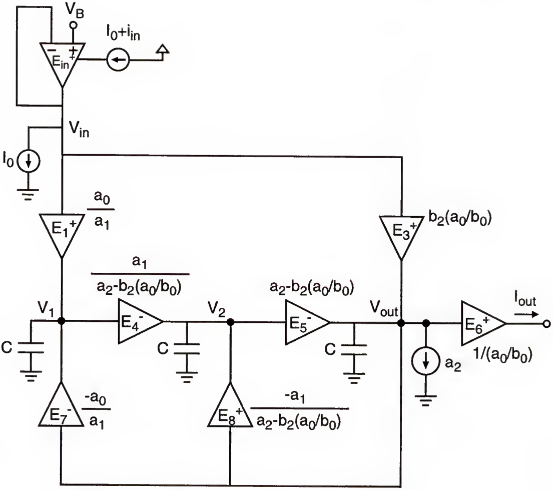


Figure 6.19 The SFG of a third-order log-domain filter with a negative weight a_2-$b_2(a_0/b_0)$.

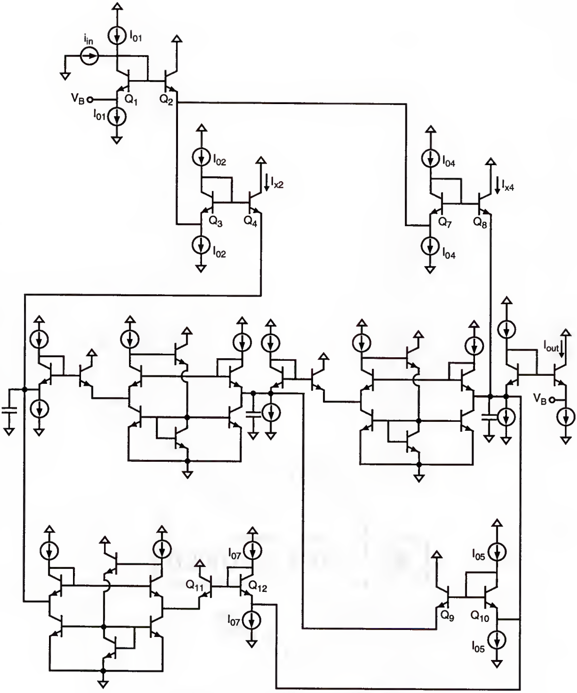


Figure 6.20 Transistor-level third-order log-domain filter based on the SFG shown in Figure 6.19.

presented that avoids the steps and leads to easily-debugged circuits. The more general approach, while more complicated, may allow simpler circuitry.

CHAPTER 7
SUMMARY AND SUGGESTIONS FOR FUTURE RESEARCH

7.1 Summary

In this dissertation, design and analysis of log-domain filters based on E cells were presented. The major contributions for the research are summarized as follows.

In Chapter 2, E cells were defined and classified into sinking and sourcing E^+ cells and E^- cells. The small-signal equivalent circuit model of an E cell was compared to that of a transconductor. A first-order log-domain filter and a log-domain integrator were designed based on E cells. E-cell-based design is a modular approach, since an E cell block can be replaced by many possible transistor-level circuits. The small-signal equivalent circuits of log-domain filters are arranged to match those of corresponding G_m-C filters.

Chapter 3 presented that, in a single-ended second-order log-domain filter, the nonlinear internal currents supplied by E cells can be much greater than bias currents even in Class A operation. Although the nonlinear internal currents are eliminated algebraically in deriving the filter transfer function, large internal currents can cause distortion by overloading transistors. Distortion mechanisms caused by internal currents were demonstrated in practical transistor-level circuits. Simple mathematical expressions were derived for predicting the peak internal currents. Simulation results matched the mathematical expressions.

Chapter 4 showed a differential second-order log-domain bandpass/ lowpass filter based on a cross-coupled log-domain integrator, and demonstrated how to add CMFB circuits to the filter without degrading external linearity. Practical but simple CMFB circuits were presented. The CMFB circuits allow closed-form solutions for nonlinear differential output currents. Also, large signal swings are allowed by the CMFB circuits, increasing the dynamic range. Three differential log-domain filters (a filter without any CMFB, a filter with geometric-mean CMFB at both bandpass and lowpass ports, and a filter with harmonic-mean CMFB at both bandpass and lowpass ports) were built in the MOSIS AMI ABN 1.5 μm CMOS process. Simulation and experimental results were given.

Chapter 5 explored the possibility of applying CMFB to only one of the two ports within a differential second-order log-domain bandpass/lowpass filter. With two integrator stages and three possible CMFB arrangements (geometric-mean CMFB, harmonic-mean CMFB, and no added CMFB) at each integrator output, nine possible combinations were implemented. Closed-form expressions were found for the peak currents in eight of the combinations (except for the combination of no added CMFB for both stages), for the case of low input frequency. In simulations of a wide variety of transistor-level of circuits implementing these filters, the HH and NH cases consistently have better dynamic range than other combinations.

Chapter 6 explored the wide variety of ways in which log-domain filters can be designed. While previous researchers have presented many seemingly novel log-domain circuit and filter topologies, this chapter demonstrated that all of these variations can be seen as simple transformation from basic underlying small-signal topologies. Several approaches to convert a current-mode G_m-C filter to a log-domain filter were compared. The approach which involves scaling the weights of the E cells in a log-domain filter SFG allows redundant circuits to be eliminated. Several options for dc biasing were compared.

7.2 Suggestions for Future Research

The following research tasks are suggested as future work regarding design and analysis of log-domain filters.

(1) The noise analysis of the differential log-domain filters with various CMFB circuits are suggested. The SNR of differential log-domain filters saturates to a maximum value of SNR for modulation indices greater than one, staying almost a constant, since the noise becomes proportional to the signal [Enz97, Pun97]. The effects of noise in CMFB circuits on the dynamic range of differential log-domain filters are needed to be explored.

(2) Other distortion mechanisms in differential log-domain filters with CMFB circuits are needed to be explored. The filters with smaller internal currents consistently have better dynamic range than the filters with larger internal currents. However, the detailed results depend strongly on the circuit implementation. Therefore, the effects of various circuit imperfections on the nonideal behavior are needed to be clarified.

REFERENCES

[Ada79] R. W. Adams, "Filtering in the log-domain," 63rd Convention A. E. S., LA, preprint 1470, May, 1979.

[Che95] Wai-Kai Chen, *The Circuits and Filters Handbook*, Boca Raton, FL: CRC Press, Inc., 1995.

[Dij98] L. P. L. van Dijk, A. C. van der Woerd, J. Mulder, and A. H. M. van Roermund, "An ultra-low-power, low-voltage electronic audio delay line for use in hearing aids," *IEEE J. Solid-State Circuits*, vol. 33, pp. 291-294, February, 1998.

[Dra97] E. M. Drakakis, A. J. Payne, and C. Toumazou, "Log-domain filters, translinear circuits and the Bernoulli cell," in *Proc. 1997 IEEE Int. Symp. Circuits Syst.*, pp. 501-504, Hong Kong, 1997.

[Dra98] E. M. Drakakis, A. J. Payne, and C. Toumazou, "Multiple feedback log-domain filters," in *Proc. 1998 IEEE Int. Symp. Circuits Syst.*, vol/ I, pp. 317-320, Monterey, CA, May, 1998.

[Dra99a] E. M. Drakakis, A. J. Payne, and C. Toumazou, "Log-domain filtering and the Bernoulli cell," *IEEE Trans. Circuits Syst., I*, vol. 46, pp. 559-571, May, 1999.

[Dra99b] E. M. Drakakis and A. J. Payne, "Structured log-domain synthesis of non-linear systems," in *Proc. 1999 IEEE Int. Symp. Circuits Syst.*, vol. II, pp. 693-696, Orlando, Florida, 1999.

[Dra00] E. M. Drakakis and A. J. Payne, "On the exact realisation of LC ladder finite transmission zeros in log-domain: a theoretical study," in *Proc. 2000 IEEE Int. Symp. Circuits Syst.*, vol. I, pp. 188-191, Geneva, Switzerland, May, 2000.

[Edw98] R. T. Edwards and G. Cauwenberghs, "A second-order log-domain bandpass filter for audio frequency applications," in *Proc. 1998 IEEE Int. Symp. Circuits Syst.*, vol. III, pp. 651-654, Monterey, CA, May, 1998.

[Elg97a] M. El-Gamal, and G. W. Roberts, "LC ladder-based synthesis of log-domain bandpass filters," in *Proc. 1997 IEEE Int. Symp. Circuits Syst.*, pp. 105-108, Hong Kong, 1997.

[Elg97b] M. El-Gamal, V. Leung, and G. W. Roberts, "Balanced log-domain filters for VHF applications," in *Proc. 1997 IEEE Int. Symp. Circuits Syst.*, pp. 493-496, Hong Kong, 1997.

[Elg98] M. El-Gamal and G. W. Roberts, "Very high-frequency log-domain bandpass filters," *IEEE Trans. Circuits Syst., II*, vol. 45, pp. 1188-1198, September, 1998.

[Elg99] M. El-Gamal and G. W. Roberts, "A 1.2 V NPN-only log-domain integrator," in *Proc. 1999 IEEE Int. Symp. Circuits Syst.*, vol. II, pp. 681-684, Orlando, Florida, May, 1999.

[Elg00a] M. El-Gamal, R. A. Baki, and A. Bar-Dor, "30-100 MHz npn-only variable-gain Class AB companding-based filters for 1.2V applications," in *Proc. 2000 IEEE Int. Solid-State Circuits Conference*, pp. 150-151, San Francisco, California, February, 2000.

[Elg00b] M. El-Gamal, R. A. Baki, and A. Bar-Dor, "30-100-MHz NPN-only variable-gain Class AB instantaneous companding filters for 1.2-V applications," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1853-1864, December, 2000.

[Enz97] C. C. Enz, M. Punzenberger, and D. Python, "Low-voltage log-domain signal processing in CMOS and BiCMOS," in *Proc. 1997 IEEE Int. Symp. Circuits Syst.*, pp. 489-492, Hong Kong, 1997.

[Enz99] C. Enz, M. Punzenberger, and D. Python, "Low-voltage log-domain signal processing in CMOS and BiCMOS," *IEEE Trans. Circuits Syst., II*, vol. 46, pp. 279-289, March, 1999.

[Fox97] R. M. Fox, M. Naharajan, and J. Harris, "Practical design of single-ended log-domain filters," in *Proc. 1997 IEEE Int. Symp. Circuits Syst.*, pp. 342-344, Hong Kong, 1997.

[Fox98] R. M. Fox, "Design-oriented analysis of log-domain circuits," *IEEE Trans. Circuits Syst., I*, vol. 45, pp. 918-921, July, 1998.

[Fox99a] R. M. Fox, H. J. Ko, W. R. Eisenstadt, "Dynamic currents in log-domain filters," in *Proc. 1999 Midwest Symp. on Circuits and Syst.*, WA1-7.2, Las Cruces, NM, August, 1999.

[Fox99b] R. M. Fox, Y. Ro, H. J. Ko, F. Yuan, K. Karnik, and W. R. Eisenstadt, "Common-mode circuits for differential log-domain filters," in *Proc. 1999 Midwest Symp. on Circuits and Syst.*, WA1-7.6, Las Cruces, NM, August, 1999.

[Fox00] R. M. Fox, "Enhancing dynamic range in differential log-domain filters based on the two-filters approach," in *Proc. 2000 IEEE Int. Symp. Circuits Syst.*, vol. 2, pp. 617-620, Geneva, Switzerland, May, 2000.

[Fox01a] R. M. Fox, H. J. Ko, W. R. Eisenstadt, "High gain common-mode feedback circuits for differential log-domain filters," in *Proc. 2001 IEEE Int. Symp. Circuits Syst.*, vol. 1, pp. 560-563, Sydney, Australia, May, 2001.

[Fox01b] R. M. Fox, H. J. Ko, W. R. Eisenstadt, "Dynamic current requirements in single-ended log-domain filters," *Anal. Integ. Circuits Sign. Proc., An Int. Jour.*, vol. 27, Issue 3, pp. 73-81, June, 2001.

[Fre93] Frey, "Log-domain filtering: An approach to current-mode filtering," *IEE Processings G*, vol. 140, pp. 406-416, December, 1993.

[Fre94] D. R. Frey, "Current mode class AB second order filter," *Electronics Lett.*, vol. 30, pp. 205-206, February 3, 1994.

[Fre96a] D. R. Frey, "Log filtering using gyrators," *Electronics Lett.*, vol. 32, pp. 26-28, January 4, 1996.

[Fre96b] D. R Frey, "Exponential state space filters: A generic current mode design strategy," *IEEE Trans. Circuits Syst., I*, vol. 43, pp. 34-42, January, 1996.

[Fre96c] D. R. Frey and L. Steigerwald, "An adaptive analog notch filter using log filtering," in *Proc. 1996 IEEE Int. Symp. Circuits Syst.*, vol. 1, pp. 297-300, Atlanta, GA, May, 1996.

[Fre96d] D. R. Frey, "Log domain filtering for RF applications," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1468-1475, October, 1996.

[Fre98] D. R. Frey, "State-space synthesis and analysis of log-domain filters," *IEEE Trans. Circuits Syst., II*, vol. 45, pp. 1205-1211, September, 1998.

[Fre99] D. R. Frey, and A. T. Tola, "A state-space formulation for externally linear Class AB dynamical circuits," *IEEE Trans. Circuits Syst., II*, vol. 46, pp. 306-314, March, 1999.

[Fre00] D. R. Frey, "C-log domain filters," in *Proc. 2000 IEEE Int. Symp. Circuits Syst.*, vol. 1, pp. 176-179, Geneva, May, 2000.

[Fri96] R. Fried, D. Python, and C. Enz, "Compact log-domain current-mode integrator with high transconductance-to-bias current ratio," *Electronics Lett.*, vol. 32, pp. 952-953, 1996.

[Geo99] T. Georgantas, S. Bouras, D. Dervenis, and Y. Papananos, "A comparison between integrated current and voltage mode filters for baseband applications," in *Proc. 1999 ICECS*, vol. 1, pp. 485-488, 1999.

[Geo01] J. Georgiou and C. Toumazou, "An operating point elimination technique for weak-inversion log-domain filters with multiple operating points," in *Proc. 2001 IEEE Int. Symp. Circuits Syst.*, tutorial guide, pp. 1.2_11-1.2_20, Sydney, Australia, May, 2001.

[Gil75] B. Gilbert, "Translinear circuits: A proposed classification," *Electronics Lett.*, vol. 11, pp. 14-16, 1975.

[Kai80] Thomas Kailath, *Linear Systems*, Englewood Cliffs, New Jersey: Prentice Hall, 1980.

[Kar00] Kiran S. Karnik, "Design of low-pass butterworth G_m-C and log-domain filters," Master's Thesis, University of Florida, 2000.

[Mul97] J. Mulder, A. C. van der Woerd, W. A. Serdijn, and A. H. M. van Roermund, "General current-mode analysis method for translinear filters," *IEEE Trans. Circuits Syst.*, I, vol. 44, pp. 193-197, March, 1997.

[Mul98] J. Mulder, M. H. L. Kouwenhoven, W. A. Serdijn, A. C. van der Woerd, and A. H. M. van Roermund, "Analysis of noise in translinear filters," in *Proc. 1998 IEEE Int. Symp. Circuits Syst.*, vol. 1, pp. 337-340, Monterey, CA, May 31-June 3, 1998.

[Per95] D. Perry and G. W. Roberts, "Log-domain filters based on LC ladder synthesis," in *Proc. 1995 IEEE Int. Symp. Circuits Syst.*, pp. 311-314, Seattle, WA, May, 1995.

[Pun95] M. Punzenberger and C. Enz, "Low-voltage companding current-mode integrators," in *Proc. 1995 IEEE Int. Symp. Circuits Syst.*, pp. 2112-2115, Seattle, WA, May, 1995.

[Pun96] M. Punzenberger and C. Enz, "A new 1.2V BiCMOS log-domain integrator for companding current mode filters," in *Proc. 1996 IEEE Int. Symp. Circuits Syst.*, vol. 1, pp. 125-128, Atlanta, GA, May, 1996.

[Pun97] M. Punzenberger and C. C. Enz, "A 1.2-V low-power BiCMOS class AB log-domain filter," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1968-1978, December, 1997.

[Pun98] M. Punzenberger and C. C. Enz, "A compact low-power BiCMOS log-domain filter," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1123-1129, July, 1998.

[Pyt99] D. Python, M. Punzenberger, and C. Enz, "A 1-V CMOS log-domain integrators," in *Proc. 1999 IEEE Int. Symp. Circuits Syst.*, pp. II 685-II 688, Orlando, FL, May, 1999.

[Pyt01] D. Python and C. C. Enz, "A micropower Class-AB CMOS log-domain filter for DECT applications," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1067-1075, July, 2001.

[Ro99] Y. Ro, "Common-mode and power supply noise rejection in low voltage analog circuits," Ph.D.'s Dissertation, University of Florida, 1999.

[See88a] E. Seevinck, *Analysis and Synthesis of Translinear Integrated Circuits*, New York: Elsevier Science Publishing Company Inc., 1988.

[See88b] E. Seevinck, W. D. Jager, and P. Buitendijk, "A low-distortion output stage with improved stability for monolithic power amplifiers," *IEEE J. Solid-State Circuits*, vol. 23, pp. 794-801, June, 1988.

[See90] E. Seevinck, "Companding current-mode integrator: a new circuit principle for continuous-time monolithic filters," *Electronics Lett.*, vol. 26, pp. 2406-2407, November, 1990.

[Ser02] F. Serra-Graells, "1V all-MOS ΣΔ A/D converters in the log-domain," in *Proc. 2002 IEEE Int. Symp. Circuits Syst.*, vol. 2, pp. 213-216, Scottsdale, AZ, May, 2002.

[Tou94] C. Toumazou, J. Ngarmnil, and T. S. Lande, "Micropower log-domain filter for electronic cochlea," *Electronics Lett.*, vol. 30, pp. 1839-1841, 1994.

[Tsi97] Y. Tsividis, "Externally linear, time-invariant systems and their application to companding signal processors," *IEEE Trans. Circuits Syst., II*, vol. 44, pp. 65-85, February, 1997.

[Wie93] Remco J. Wiegerink, *Analysis and Synthesis of MOS Translinear Circuits*, Norwell, MA: Kluwer Academic Publishers, 1993.

[Wu98] J. Wu and E. I. El-Masry, "New fully balanced log-domain integrators," in *Proc. 1998 IEEE Int. Symp. Circuits Syst.*, vol. 1, pp. 313-316, Monterey, CA, May 31-June 3, 1998.

[Yan96] F. Yang, C. Enz, and G. Van Ruymbeke, "Design of low-power and low-voltage log-domain filters," in *Proc. 1996 IEEE Int. Symp. Circuits Syst.*, pp. 117-120, Atlanta, GA, May, 1996.

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